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**Nonlinear Analysis of Power Systems including
FACTS and Custom Power Devices Based on
Bifurcation Theory and Newton Methods**

by

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THESIS

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ac capacitor	C_{ac}
Adjustable System Drive	ASD
Amplitude modulation ratio	m_a
Aprille and Trick Method	AT
Average load power	P_l^{av}
Average voltage across the dc capacitor	v_{dc}^{av}
Brute Force	BF
Capacitance	C
Compensation voltage injected by the DVR	V_f
Custom Power	CP
Cutoff Frequency	Ω_c
dc capacitor	C_{dc}
Derivative respect to time of a function $f(\mathbf{x},t)$	$df(\mathbf{x},t)/dt$
Direct Approach	DA
Direct axis	d
Discrete Exponential Expansion Method	DEE
Discrete transition matrix	Φ_k
Distribution Static Compensator	DSTATCOM
Dynamic Voltage Regulator	DVR
Electric Arc Furnace	EAF
Electrical output torque	T_e
Enhanced Numerical Differentiation Method	END
Exponential function	e
Finite Differences Method	FD
Fixed Capacitor	FC
Flexible ac Transmission Systems	FACTS
Flux linkage ($i=q$ or d and $j=s$ or r)	λ_{ij}
Fourth-order Runge-Kutta	RK4
Frequency modulation ratio	m_f
Fundamental component of v_{ix} , for $x = a, b, c$	v_{tfx}
High Voltage Direct Current Light	HVDC Light
High Voltage Direct Current Transmission	HVDC
Hysteresis Band	h
Identity matrix	\mathbf{I}
Inductance	L
Infinite	∞
Instantaneous active power	P
Instantaneous current source	i_s
Instantaneous current	i
Instantaneous load current	i_l
Instantaneous power losses	P_{loss}

Instantaneous reactive power	Q
Instantaneous terminal voltage	v_t
Instantaneous voltage source	v_s
Instantaneous voltage	v
Integral gain of the load voltage in the DVR	$K_{i\phi}$
Integral gain of the power factor controller	$K_{i\beta}$
Integral gain of voltage controller of dc capacitor	K_{idc}
Integration operator	\int
Jacobian	$\mathbf{J}(t)$
Load torque	T_L (or T_I)
Load voltage (phasor)	\mathbf{V}_l
Load voltage magnitude	$ V_l $
Load voltage reference magnitude	$ V_l^{ref} $
Magnetic flux	λ
Magnitude of the current source	$ I_s $
Magnitude of the load current	$ I_l $
Magnitude of the terminal voltage	$ V_t $
Magnitude of the voltage at the converter terminals of the DVR	$ V_{inj} $
Magnitude of the voltage source	$ V_s $
Magnitude	$ \quad $
Mismatch	Δ
Moment of inertia	J
Number of Full Cycles	NFC
Number of poles	p
Numerical Differentiation Method	ND
Ordinary Differential Equations	ODEs
Period	T
Point Common Coupling	PCC
Proportional gain of the load voltage in the DVR	$K_{p\phi}$
Proportional gain of the power factor controller	$K_{p\beta}$
Proportional gain of voltage controller of dc capacitor	K_{pdc}
q and d axis magnetizing flux linkages	$\lambda_{mq}, \lambda_{md}$, respectively
q and d axis rotor currents	i_{qr}, i_{dr} , respectively
q and d axis rotor voltages	v_{qr}, v_{dr} , respectively
q and d axis stator currents	i_{qs}, i_{ds} , respectively
q and d axis stator voltages	v_{qs}, v_{ds} , respectively
Quadrature axis	q
Reference compensator currents	i_f^*
Reference dc voltage	v_{dc}^*
Resistance	R
Rotor angular electrical speed	ω_r
Rotor axis	r
Rotor leakage reactance ($\omega_e L_{lr}$)	X_{lr}
Rotor resistance	R_r

State variables at the beginning of the base cycle	\mathbf{x}^i
State variables at the end of the base cycle	\mathbf{x}^{i+1}
State variables at the limit cycle	\mathbf{x}^∞
Static Synchronous Compensator	STATCOM
Static Synchronous Series compensator	SSSC
Static Var Compensator	SVC
Stator angular electrical base frequency	ω_b
Stator angular electrical frequency	ω_e
Stator axis	s
Stator leakage reactance ($\omega_e L_{ls}$)	X_{ls}
Stator resistance	R_s
Switching function	S
Terminal voltage (phasor)	V_t
Thyristor Controlled Reactors	TCR
Thyristor Controlled Series Compensator	TCSC
Thyristor Switch Capacitor	TSC
Time	t
Transition matrix	Φ
Trapezoidal Rule	TR
Unified Power Flow Controller	UPFC
Unified Power Quality Conditioner	UPQC
Voltage at the converter terminals of the DVR	v_{inj}

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List of Publications

The following publications are associated with this research work:

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- 1) Segundo-Ramírez, J., and Medina, A. “*Periodic Steady-State Solution of Electric Systems Including UPFCs by Extrapolation to the Limit Cycle.*” *IEEE Transaction on Power Delivery*, vol. 23, no. 3 (July 2008): 1506 - 1512. Impact Factor: 1.289.
- 2) Segundo-Ramírez, J., Medina, A., Ghosh, A. and Ledwich, G. “*Stability Analysis Based on Bifurcation Theory of the DSTATCOM Operating in Current Control Mode.*” *IEEE Transaction on Power Delivery*, vol. 24, no. 3 (July 2009): 1670-1678. Impact Factor: 1.289.
- 3) Segundo-Ramírez, J., and Medina, A. “*Modeling of FACTS Devices Based on SPWM VSCs.*” *IEEE Transaction on Power Delivery*, vol. 24, no. 4 (October 2009): 1815-1823. Impact Factor: 1.289.
- 4) Segundo-Ramírez, J., and Medina, A. “*Computation of the Steady-State Solution of Nonlinear Power Systems by Extrapolation to the Limit Cycle Using a Discrete Exponential Expansion Method.*” *International Journal of Nonlinear Sciences and Numerical Simulation*, 2009. (Accepted). Impact Factor: 8.479.
- 5) Segundo-Ramírez, J., and Medina, A. “*An Enhanced Process for the Fast Periodic Steady State Solution of Nonlinear Systems by Poincaré Map and Extrapolation to the Limit Cycle.*” *International Journal of Nonlinear Sciences and Numerical Simulation*, 2009. (Accepted). Impact Factor: 8.479.
- 6) Segundo-Ramírez, J., Medina, A., Ghosh, A. and Ledwich, G. “*Nonlinear Oscillations Assessment of the DSTATCOM Operating in Voltage Control Mode.*” *Electric Power Components and Systems*,” (Accepted). Impact Factor: 0.376.
- 7) Ramos-Carranza, A. Medina, A. Segundo-Ramírez, J. and Madrigal, M. “*Shunt Hybrid Filter Control for Harmonic Current Mitigation and Reactive Power Compensation in Electric Systems.*” *Transaction on Power Delivery* (Under review). Impact Factor: 1.289.
- 8) Segundo-Ramírez, J., Medina, A., Ghosh, A. and Ledwich, G. “*Stability Analysis Based on Bifurcation Theory and Continuation Techniques of a Capacitor-Supported DVR Including Harmonic Distortion.*” *Transaction on Power Delivery* (Under review). Impact Factor: 1.289.

Segundo-Ramírez, J., Bárcenas, E., Medina, A., and Cárdenas, V. “*Steady-State and Dynamic State-Space Model for Efficient Solution and Stability Assessment of ASDs.*” (To be submitted)

Conference Papers:

- 1) Segundo-Ramírez, J., and Medina, A. “Periodic Steady State Solution of Electric Systems Including UPFCs.” *PES General Meeting*, July 2008: 1-1.
- 2) Segundo-Ramírez, J., and A. Medina. "Transient and Steady-State Analysis of the UPFC Using a Fourier Series Approach Model." 13th International Conference on Harmonics and Power Quality. Wollongong, 2008. 1-6.
- 3) Segundo-Ramírez, J., and A. Medina. “Periodic Steady State Solution of FACTS Devices Based on SPWM VSCs.” *IEEE ISIE 2009*, 5-8 July 2009: 1644-1649.

Abstract

This thesis presents the modeling of electric power systems including FACTS and Custom Power (CP) devices and their stability analysis through application of bifurcation theory, continuation methods, and Newton methods to compute the periodic steady state.

The previous stability analyses of FACTS and Custom Power devices based on bifurcation theory using continuation methods neglected the harmonic distortion introduced by the voltage source converter (VSC). Besides, the network transients have not been taken into account. Under this formulation, the electric power network was modeled through a phasor representation, and obviously, only the fundamental frequency was considered in those analyses.

In this research, two VSC models based on Fourier series and hyperbolic tangent function are proposed. The proposed models can be used for fast simulation in the time domain of power-electronic devices based on sinusoidal pulse-width modulation VSCs; the undesirable error introduced by the high commutates rates are removed; even though the harmonic distortion coming from the converter is taken into account. The switching instants in the Fourier model are approximated in a closed form, and an iterative algorithm based on the Newton-Raphson method is developed for the exact calculation of the switching instants. The hyperbolic tangent model does not need the calculation of the switching instants as in the case of the Fourier model. With these VSC's models the computation of the periodic steady-state solution of power systems including FACTS is efficiently obtained by extrapolation to the limit cycle using a Newton method. In addition, it is possible to assess the stability through the Floquet multiplier. Two Newton methods to compute efficiently the periodic steady state solution are presented. One is based on an Enhanced Numerical Differentiation technique, and the other one is based on Discrete Exponential Expansion approach of the transition matrix. These methods prove to be more efficient than the conventional methods such as [Aprille Jr. and Trick 1972], [Colon and Trick 1973], and [Semlyen and Medina 1995]. It is also presented the stability analysis for a distribution static compensator (DSTATCOM) that operates in current control mode and voltage control mode based on bifurcation theory. A control design for the DSTATCOM is proposed. Along with this control, a suitable mathematical representation of the DSTATCOM is proposed. In addition, the stability analysis for a capacitor-supported dynamic voltage restorer (DVR) based on bifurcation theory and a continuation method is presented. The stability regions in the Thevenin equivalent plane are computed for different operating scenarios. In addition, the stability regions in the control gain space, as well as the contour lines for different Floquet multipliers are computed.

The proposed models and analysis are validated against the solution obtained with the power system blockset of Simulink and with PSCAD/EMTDC. Additionally, the proposed VSC models based on the Fourier series and the hyperbolic tangent approach are validated against the response obtained by measurements from a 1.5 kVA ASD experimental setup system.

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1 Introduction

Flexible ac Transmission Systems (FACTS), provide higher controllability in power systems by means of power electronic devices. Several FACTS devices have been already introduced for various applications worldwide. A number of new types of devices are in the stage of being introduced in practice. Even more concepts of configurations of FACTS-devices are discussed in research and literature. FACTS technology provides a better ability to varying operational conditions and improve the usage of existing installations.

1.1 State of the Art

It can be seen that with growing line length and with higher power demand the opportunity for FACTS devices gets more important. The devices work electrically as fast current, voltage or impedance controllers. The power electronic allows very short reaction times down to far below one second (\sim ms). Detailed introductions in FACTS devices can also be found in the literature [Hingorani and Gyudyi 2000] [Sood 2004] [Acha, et al. 2004] [Mathur and Varma 2002] [Padiyar 2007] [Zhang, et al. 2006] with the main focus on basic technology, modeling and control.

Basically, there are two groups of FACTS, one is based on thyristor valve operation [Hingorani and Gyudyi 2000], and the other is based on Voltage Source Converters (VSCs) [Segundo-Ramírez and Medina 2008] [Segundo-Ramírez and Medina 2009]. A list of some FACTS devices are shown in Table 1.1.

TABLE 1.1 OVERVIEW OF THE PRINCIPAL FACTS-DEVICES

Connection Type	FACTS Devices	
	Thyristor-Based FACTS	VSC-Based FACTS
Shunt Connected	Static Var Compensator (SVC)	Static Compensator (STATCOM)
Series Connected	Thyristor Controlled Series Compensator (TCSC)	Static Series Synchronous Compensator (SSSC)
Shunt and Series Connected	HVDC	Unified Power Flow Controller (UPFC)
		HVDC VSC

The FACTS devices based on VSCs provide a controllable voltage magnitude and phase angle due to a Pulse Width Modulation (PWM) technique [Mohan, et al. 1995]. The Static Compensator (STATCOM) [Hingorani and Gyudyi 2000] is a shunt connected device that is able to provide reactive power support at a network location far away from the generators. Through this reactive power injection, the STATCOM can regulate the voltage at the connection node. The Static Synchronous Series compensator (SSSC) [Hingorani and Gyudyi 2000] is a series device which injects a voltage in series with the transmission line. The Unified Power Flow Controller (UPFC) [Hingorani and Gyudyi 2000] is the most versatile device of the family of FACTS devices, since it is able to control the active and the reactive power, respectively, as well as the voltage at the connection node. In Figure 1.1 a schematic representation of the STATCOM, the SSSC, and the UPFC are presented. The mathematical representation adopted in this thesis is the state space approach of non-autonomous nonlinear ODE sets periodically forced, where the electric transients and the harmonic distortion are not neglected. Additionally, all the state variables are in instantaneous values, thus the steady-state solution is a limit cycle. In the conventional stability analysis of power systems including FACTS and CP devices [Srivastava and Srivastava 1998], the power system is represented using Root Mean Square (RMS) quantities, and the network transients are neglected

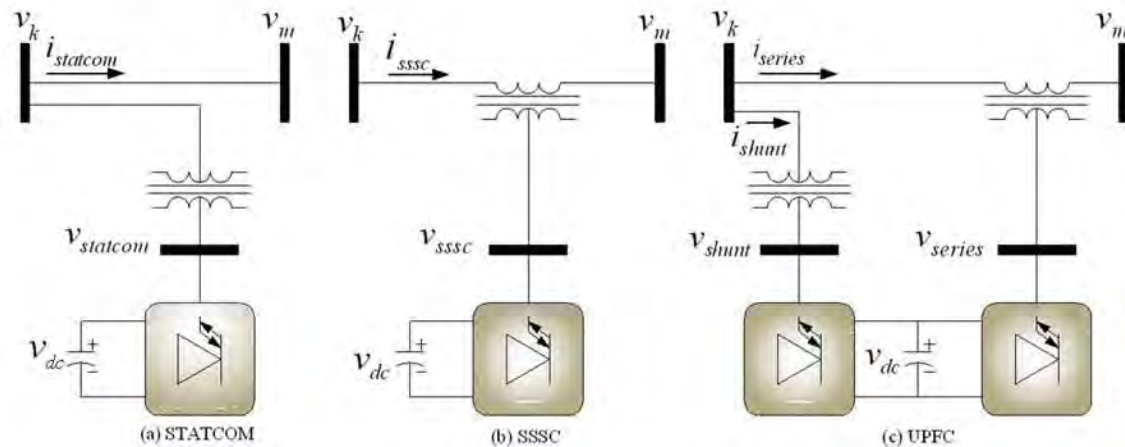


Figure 1.1 FACTS devices based on VSCs. (a) STATCOM, (b) SSSC, and (c) UPFC

To explore both stable and unstable limit cycles [Parker and Chua 1989], the bifurcation analysis is used; a nonlinear mathematical theory [Parker and Chua 1989] [Nayfeh and Balachandran 1995] used to qualitatively investigate how the integral curves change as the parameters are varied. The bifurcation theory has been applied to the analysis of voltage collapse [Dobson and Chiang 1989], analysis of the Electric Arc Furnace (EAF) [Medina, et al. 2005], chaotic oscillations [Wang, et al. 1994], ferroresonance analysis [Wörnle, et al. 2005], and the design of nonlinear controllers [Lee, et al. 2001]. It has also been applied to assess the dynamic behaviour of nonlinear components such as induction motors [Rosehart and Cañizares 1999], load models [Cañizares 1995] [Pai, et al. 1995], tap changing transformers [Vu and Liu 1989], and FACTS devices [Srivastava and Srivastava 1998] [Mithulananthan, et al. 2003].

In power electronic, the bifurcation theory has been used successfully to analyze the stability of power converters and switched circuits [Azzouz, et al. 1983] [Zhusubaliyev and

Mosekilde 2006] [Jalali, et al. 1996] [di Bernardo and Vasca 2000] [di Bernardo, et al. 1998] [lu and Robert 2003] [Tse 2004] [Deane and Hamill 1990]. Conventionally, this analysis is carried-out with the discrete-time iterative mapping approach [Zhusubaliyev and Mosekilde 2006] [Jalali, et al. 1996] [di Bernardo and Vasca 2000] [di Bernardo, Garofalo, et al. 1998] [lu and Robert 2003] [Tse 2004]. Under this approach, the switching converter is essentially modeled as piecewise switched circuits. This results in a nonlinear time-varying operating mode, which naturally demands the use of nonlinear theory [Tse 2004]. In the discrete-time iterative mapping approach, it is assumed that between switching instants, the network is linear time-invariant. Thus, the solution between switches can be found in a closed-form. Here, the nonlinearity comes from the switching control.

The previous stability analyses of FACTS and Custom Power devices based on bifurcation theory using continuation methods neglected the harmonic distortion introduced by the voltage source converter (VSC). Besides, the network transients have not been taken into account. Under this formulation, the electric power network was modeled through a phasor representation, and obviously, only the fundamental frequency was considered in those analyses.

The compensating FACTS devices based on VSCs, under analysis in this investigation are briefly described below.

1.1.1 Static Compensator (STATCOM)

It is a shunt device that does not require passive elements for reactive compensation. The STATCOM operation is based on a VSC, which is supplied by a dc storage capacitor. The VSC terminals are connected to the dc system through a coupling transformer. The VSC produces a quasi-sine wave voltage at the fundamental frequency (50 or 60 Hz). The STATCOM can generate or absorb reactive power. A schematic representation of the STATCOM is shown in Figure 1.1(a).

Assuming that the losses in the VSC and the coupling transformer are negligible, $v_{statcom}$ is in phase with the voltage at the terminal bus v_k . In this situation, the current $i_{statcom}$ is completely reactive. If the magnitude of the voltage v_k is more than the magnitude of $v_{statcom}$, the reactive current flows from the bus to the VSC, which means that the STATCOM absorbs reactive power. On the other hand, if the magnitude of $v_{statcom}$ is more than the magnitude of v_k , the reactive current flows from the VSC to the ac system. Then, the STATCOM injects reactive power to the system. In practice, the power losses of the STATCOM are not negligible and must be drawn from the ac system to maintain constant the dc capacitor voltage.

1.1.2 Static Synchronous Series Compensator (SSSC)

The SSSC is a series device in which a synchronous voltage source injects a fundamental frequency voltage in series with the transmission line through a coupling transformer. The synchronous voltage source is supplied by a VSC. A schematic representation of the SSSC is shown in Figure 1.1(b)

Ideally, the injected voltage is in quadrature with the line current. In this mode the VSC does not absorb or generate any real power. However, in practice, the VSC losses must be

replenished by the ac system, in consequence a small phase lag is introduced for this purpose. There are two modes of operation of this device, one is in which the injected voltage is proportional to the line current and the other in which the injected voltage is independent of the line current [Gyugyi, et al. 1997]. The operating characteristics make this device very attractive for power transmission application. The main limitation of application is due to the losses and cost of the converter. The SSSC is a device which has so far not been built at transmission level because Series Compensator (fixed capacitor) and TCSC [Hingorani and Gyudyi 2000] are fulfilling all the today's operational requirements and a lower cost.

1.1.3 Unified Power Flow Controller (UPFC)

This device contains two VSCs connected together through a dc link storage capacitor. One of the VSCs is connected in series with the transmission line, while the other VSC is connected in shunt with the transmission line. The UPFC can control the active and reactive power flow in the transmission line, and at the same time can regulate the voltage magnitude at the connection node. To control the real and reactive power flow in the series side, the UPFC allows interchange of real power between the shunt and the series converters. The main disadvantage of this device is the high cost level due to the complex systems setup [Zhang, et al. 2006]. A schematic representation of the UPFC is shown in Figure 1.1(c).

1.1.4 Other FACTS Devices

1.1.4.1 Static Var Compensator (SVC)

The Static Var Compensators are mainly used in power systems for voltage control. Some other application can be achieved, for example, for stabilization of power oscillations, or for improving transient stability [Hingorani and Gyudyi 2000] [Zhang, et al. 2006].

The SVC behaves like a shunt-connected variable reactance, which generates or absorbs reactive power in order to regulate the voltage magnitude at the point of connection to the ac network. The thyristor's firing angle control enables the SVC to swiftly respond

There are two main building blocks for SVCs; Thyristor Switched Capacitor (TSC) and Thyristor Controlled Reactor (TCR). The TSC is shown in Figure 1.2(a). In this configuration, a capacitor is connected in series with two opposite poled thyristors. Current flows through the device can be stopped by blocking the thyristors, and as a consequence the TCS behaves like a variable capacitive reactance. In practical applications, the TCS always comes in a group as shown in Figure 1.2(b).

A TCR is a reactor connected in series with two opposite poled thyristors. A schematic diagram of a TCR is shown in Figure 1.3. The firing signal for each thyristor is delayed by an angle α from the zero crossing of the v_s . This angle, often called conduction angle, is shown in Figure 1.4. This Figure shows the typical TCR steady state voltage-current waveform. Conduction angle must be between 90° and 180° . Observe that for $\alpha=90^\circ$, the

current waveform will be continuous and purely sinusoidal, and for $\alpha = 180^\circ$, the current will be zero.

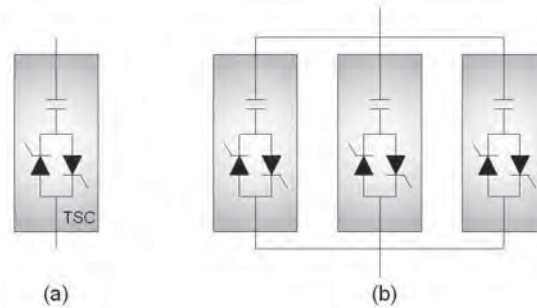


Figure 1.2 (a) Schematic diagram of a TSC, and (b) multiple TSC connection

A practical SVC frequently contains both TCS modules and TCR, as shown in Figure 1.5. In addition, the SVC would contain a Fixed Capacitor (FC). The tuned filters are included to suppress harmonic current flowing into the ac system. The SVC contains firing and control circuits. The SVC is connected in shunt to an ac line through a step down transformer. The SVC is placed in the middle of the transmission line for line power and voltage regulation [Gyudyi 1988]. The SVCs can be placed close to loads to provide voltage support at the load bus, thereby avoiding possible voltage instability.

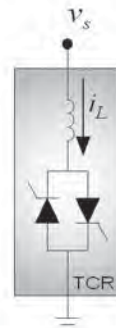


Figure 1.3 Schematic diagram of a TCR

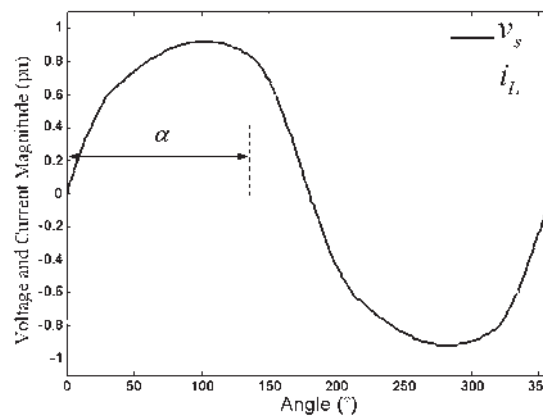


Figure 1.4 Steady state voltage-current waveform of a TCR

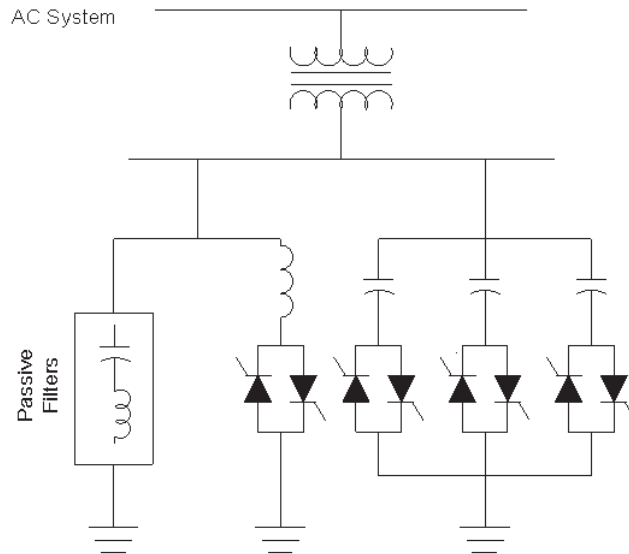


Figure 1.5 SVC connected to an ac network

1.1.4.2 Thyristor Controlled Series Compensator (TCSC)

The Thyristor Controller Series Capacitor [Kinney, et al. 1995] [Hingorani and Gyudyi 2000] contains an ac Fixed Capacitor (FC) that is connected in parallel with a TCR. A schematic representation of the TCSC is shown in Figure 1.6.

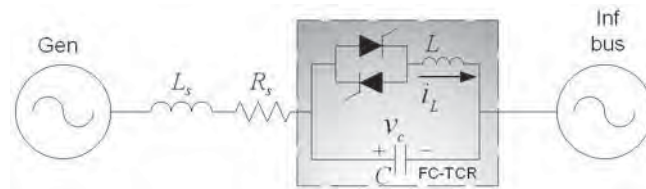


Figure 1.6 Schematic Representation of a TCSC

Since this is a series compensation device, its placement is not that crucial and it can be placed anywhere along the line. The equivalent reactance of the parallel combination of a TCR with a fundamental reactance of $X_L(\alpha)$ and a capacitance with a reactance of X_C is given by,

$$X_{eq}(\alpha) = \frac{X_C X_L(\alpha)}{X_C - X_L(\alpha)} \quad (1.1)$$

It can be noticed from (1.1) that by varying $X_L(\alpha)$ the equivalent reactance can be inductive or capacitive. The gating signal of each thyristor is delayed by a firing angle α , from the zero crossing of v_c . There are many ways of computing the fundamental frequency reactance of $X_L(\alpha)$ [Christl, et al. 1992] [Fuerte-Esquivel, et al. 2000]. The voltage-current characteristic of the TCSC is very similar to that shown in Figure 1.4.

The variation of per-unit TCSC reactance, X_{eq} , as a function of the firing angle α , is shown in Figure 1.7.

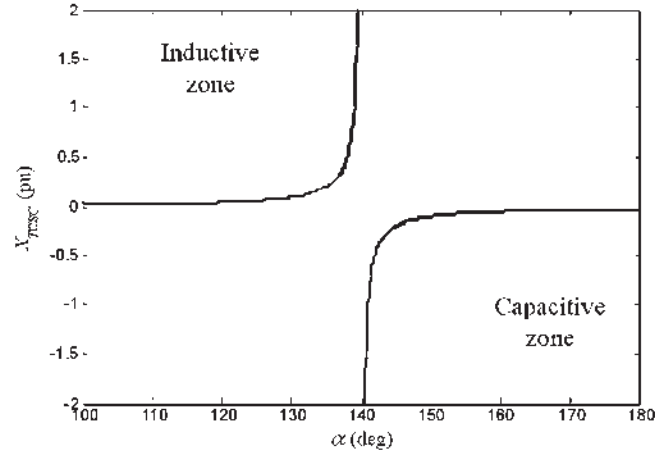


Figure 1.7 Variation of TCSC reactance with the firing angle

1.1.4.3 High Voltage Direct Current (HVDC) Transmission

The application of power electronics in power systems started with bulk power transmission through High Voltage Direct Current. The schematic diagram of a double-poled HVDC transmission system linking two ac systems is shown in Figure 1.8. One of these converters is for the positive pole, and the other for the negative pole. The converters are thyristors built and are supplied from the three-phase ac side through transformers. In addition, at the point of coupling of the ac system and the dc system, tuned ac filters are connected so that harmonics generated by the converters do not flow into the ac systems. On the dc side a smoothing inductor L_s is connected to the output of each converter to smooth the ripples in the dc current; dc filters are also provided to cancel-out harmonics from traveling down the dc transmission line. The direction of the power transfer can be reversed as well by changing the operating principle of the converters.

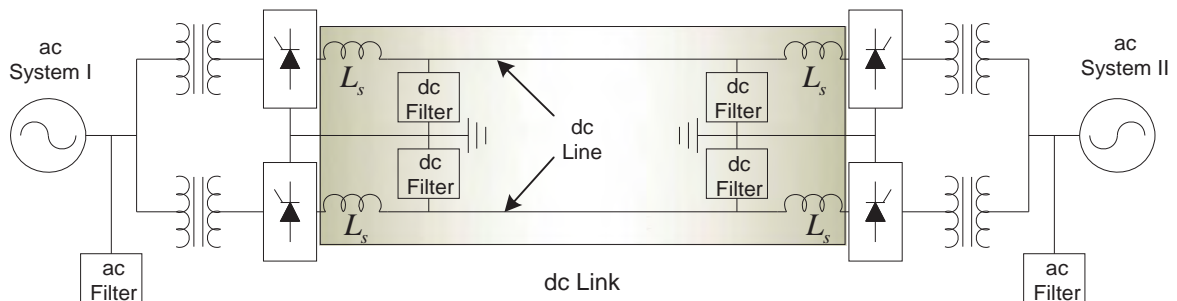


Figure 1.8 A double-poled Thyristor-Based HVDC Link

1.1.4.4 High Voltage Direct Current (HVDC) Light

Derived from the Thyristor-Based HVDC is the HVDC Light technology, which uses Insulated Gate Bipolar Transistors (IGBTs); the IGBTs constitute the VSCs. The converters are operated under a PWM technique. Under this modulation technique, it is possible to almost instantaneously create any phase and/or amplitude of the voltage at the terminals of the converters, which are connected to the ac system. The use of PWM VSC-based HVDC offers the possibility of controlling both active and reactive power flow independently. This has many technical and economical characteristics, which make it an ideal candidate for a

variety of transmission applications where the conventional HVDC is unable to compete. It is said that it has brought down the economical power range of HVDC transmission to only a few megawatts. At present, the technology enables power rating up to 300 MW. In the simplest form, it comprises two STATCOMs linked by a dc cable, as illustrated in Figure 1.9 [Acha, et al. 2002].

HVDC light uses cables that can be buried under the ground. Unlike the overhead lines, the cables are not subjected to storms, snow and ice and there is not right of way problem either. It is therefore claimed that the HVDC light is a technology for the future dc transmission [Ghosh and Ledwich 2002].

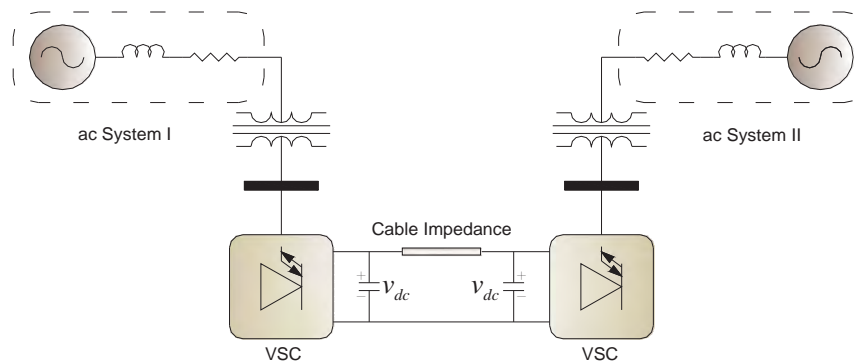


Figure 1.9 A VSC-Based HVDC Link

1.2 Power Electronic Application in Distribution Systems

In analogous way, the devices based on power electronics are also used in the distribution systems to increase the reliability and the power quality provided to the end users. This technology is called Custom Power [Hingorani 1995] [Ghosh and Ledwich 2002]. With this technology the electrical companies can provide a service of better quality and higher reliability. The CP devices provide an integral solution to the problems that are facing the electrical companies in the distribution of power, since this technology improves the service in terms of the reduction of interruptions and voltage variation. In early days, the power quality was referred to the continuity in the service, at acceptable voltage magnitude and frequency. However, the increase of nonlinear loads such as computers, microprocessors, and power electronic systems has resulted in new power quality issues. These nonlinear loads cause power quality problems, and are very sensitive to voltage variations as well.

These devices are categorized into two broad classes; network reconfiguring devices and compensating devices. The network reconfiguring devices include Static Current Limiter (SCL), Static Circuit Breaker (SCB), Static Transfer Switch (STS) [Ghosh and Ledwich 2002].

This thesis is only focused on the compensating devices. These are detailed next.

1.2.1 Distribution Static Compensator (DSTATCOM)

This it is a shunt connected device that has the same structure that the STATCOM [Ghosh and Ledwich 2002]. The DSTATCOM can compensate the load, correct the power factor and reduce the harmonic content in the network. This device can even regulate the voltage at the connection bus. There are important differences between the STATCOM and the DSTATCOM. The STATCOM injects almost sinusoidal a balanced three-phase current, whereas the DSTATCOM must be able to inject an unbalanced and harmonically distorted current in order to balance and to eliminate the harmonic distortion in the source current. Therefore, the compensation algorithm and the control are significantly different between DSTATCOM and STATCOM.

There are two operating modes of the DSTATCOM. The difference is associated to its control and its compensation algorithm. These operating modes are the voltage and current modes, respectively.

1.2.1.1 DSTATCOM Operating in Current Control Mode.

In the current control mode, the DSTATCOM compensates for any unbalance or distortion in the load, thus, the load draws a balanced current from the system irrespective of any unbalance or harmonic distortion in the load [Ghosh and Ledwich 2003]. One of the most important issues for the load compensation is the generation of the reference compensator currents. There are several techniques proposed; [Ghosh and Ledwich 2003], [Ghosh and Joshi 1998], [Akagi, et al. 1984], [Akagi, et al. 1986], [Ghosh and Joshi 2000] and [Mishra, et al. 2003]. However, most of these methods assume that the voltage at the Point Common Coupling (PCC) is stiff. Unfortunately this is not a valid assumption for most practical applications. In [Ghosh and Ledwich 2003] and [Mishra, et al. 2003] some algorithms that take into account the feeder impedance are proposed.

The schematic diagram of a distribution system compensated by an ideal DSTATCOM is shown in Figure 1.10. The DSTATCOM is operating in current control mode and behaves ideally as a current source i_f . It is assumed that the Load-2 is reactive, unbalanced and nonlinear. In absence of the compensator, the source current will be unbalanced and distorted, and consequently, so will be the voltage at node 1. The compensator must be operated in such a way that it does not inject or absorb any real power in steady state.

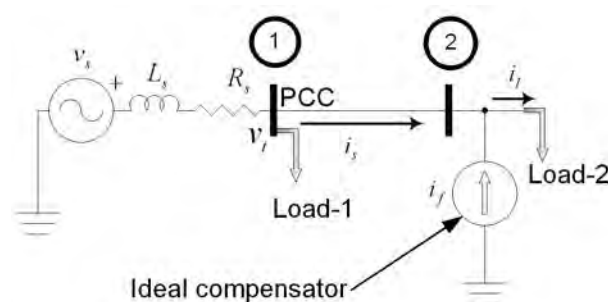


Figure 1.10 Schematic diagram of load compensating using DSTATCOM

In order to mitigate this problem, the DSTATCOM injects a different current, so that the current i_s becomes fundamental and balanced. In addition, the DSTATCOM can force the current i_s to be in phase with the voltage at node 2.

1.2.1.2 DSTATCOM Operating in Voltage Control Mode.

A schematic diagram of an ideal DSTATCOM acting as a voltage regulator is shown in Figure 1.11. In this ideal representation, the DSTATCOM behaves as a voltage source connected to the PCC. The voltage regulation is carried-out by injecting a set of three currents i_d in such a way that the voltage v_t follows a specified reference. In steady state the DSTATCOM does not interchange any real power. The magnitude of the reference voltage can be arbitrarily chosen, and its phase is chosen in such a way that the source current is equal to the p component of the load current i_l . It is assumed that i_l is unbalanced, and harmonic distorted. In absence of the compensator, $i_s=i_l$, consequently, i_s is also unbalanced and harmonic distorted. Besides, v_t is unbalanced and distorted.

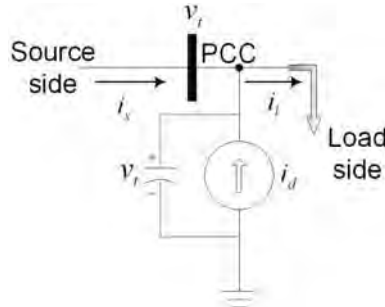


Figure 1.11 Schematic diagram of voltage regulating using DSTATCOM

1.2.2 Dynamic Voltage Restorer (DVR)

The DVR has been proposed to protect critical and sensitive loads from supply-side disturbances, except outages [Ghosh and Ledwich 2002]. It is connected in series with a distribution feeder and is capable of generating or absorbing real and reactive power at its ac terminals. The operation principle of the DVR is simple; it injects a voltage in series with the feeder. Ideally, this injected voltage is in quadrature with the line current so that the DVR behaves like an inductor or a capacitor for the purpose of increasing or reducing the overall reactive voltage drop across the feeder. In this operating mode, the DVR does not have any interchange of real power with the system in steady-state. The DVR can restore the load-side voltage to the desired amplitude and waveform even when the source voltage is unbalanced and distorted. A schematic representation of the DVR is shown in Figure 1.12.

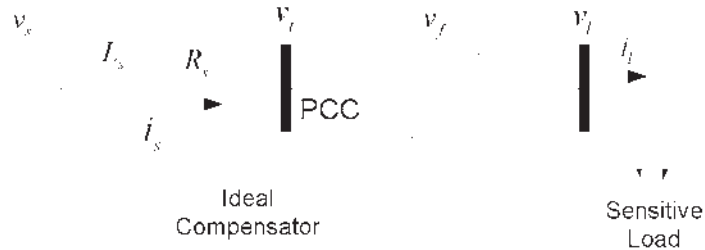


Figure 1.12 Schematic diagram of voltage regulating using DVR

This series connected device has the same structure that the SSSC. Although DVR and SSSC have almost the same structure their principles of operation considerably differ. Whereas the SSSC injects a balanced three-phase voltage in series, the DVR has to be able to inject unbalance three-phase voltage to maintain the load voltage balanced and sinusoidal at the specific magnitude,. In addition, in case of distorted source voltage, the DVR has to be able to inject a distorted voltage to compensate the harmonic distortion of the source voltage.

1.2.3 Unified Power Quality Compensator (UPQC)

This device has the same structure of the UPFC. The UPQC is the most versatile compensating device of the family of CP technology, since it can simultaneously inject current in parallel and voltage in series. As the DSTATCOM and the DVR, the UPQC must be able to inject distorted and unbalanced voltages and currents. It is stipulated that the UPQC should perform the following functions: The series VSC must inject a voltage, so that the voltage at the critical load bus remains balanced, sinusoidal, with pre-specified magnitude and phase angle. The shunt VSC must eliminate unbalance and harmonics from the PCC voltage.

The UPQC connected in a distribution system is shown in Figure 1.13. The UPQC combines the series voltage v_d and the shunt current i_f . The voltage v_d forced the load voltage to be a balanced sinusoid, irrespective of unbalance or distortion in the terminal voltage v_t . On the other hand, the shunt current i_f forces the source current i_s to be a balanced sinusoid irrespective of the load current i_l .

The UPQC can bear short interruptions and critical sags and swells, meanwhile, the DSTATCOM operating in voltage mode and the DVR can only compensate small sags and swell in magnitude and duration. Even in the case where the DVR is rectifier supported, it cannot properly compensate interruptions and critical voltage variations. In addition, the UPQC can regulate the voltage magnitude and phase at the load bus.

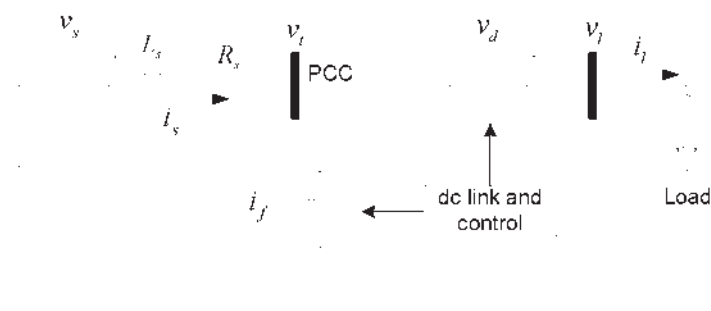


Figure 1.13 Schematic representation of UPQC connected in a distribution system

1.3 Motivation Behind the Present Research

Reliability and quality are the two most important aspects in power systems operation. A power system is reliable if customers always get interruption-free power. The term power quality is often referred to as maintaining near sinusoidal voltage at the stipulated magnitude and frequency at all times. Maintaining levels and frequency are the

responsibility of generation; however, it does not mean that the customers get quality power, even if the generation quality levels are properly met.

From the operation point of view, the FACTS and CP technology is concerned with the ability to control the electric variables in the power network in different ways that were not possible until the advent of the power electronic technology in power systems. However, undesirable nonlinear phenomena related to these devices connected in the electric network emerge and must be analyzed. These problems are presented in the electric network as adverse power quality effects and nonlinear oscillations [Guckenheimer and Holmes 1990], which delimit the practical operating points, since out of these limits the electric system loses its stability.

The common adopted technique to analyze the stability in electric network including FACTS or/and CP devices is the brute force approach or eigen-analysis [Kundur 1994] [Ghosh and Ledwich 2002]. The brute force method is based on the direct application of a numerical integration method to investigate the trajectories of the state variables. However, this method is limited to the investigation of asymptotically stable steady states. In the eigen-analysis, the system is linearized around an equilibrium operating point. The stability of this point is determined by computing its eigenvalues. However, in this conventional stability analysis, the power system is represented in RMS quantities, and the network transients are neglected. This approach is frequently used due to its simplicity. However, there are evident limitations since the harmonic distortion introduced into the power system by the FACTS and CP devices is neglected.

The operation of the FACTS and CP devices produces an excellent controllability of the power flows; unfortunately, they also introduce undesirable effects in the nodal voltage and current waveforms of the power network such as harmonic distortion. The understanding of the harmonic interaction between this device and the network, as well as its impact in the system, can be obtained from an accurate mathematical model of these devices. These models can give a clear perception about the performance of these devices, as well as the possibility to determinate the harmonic distortion produced by a particular device and to assess its adverse operation impact. In addition, a Newton method for the fast computation in the time domain of the periodic steady state solution of power networks including FACTS and CP is necessary.

In this investigation, the power system is represented through instantaneous quantities, the network transients are taken into account and the electric sources voltage are assumed to be sinusoidal. In particular, it is difficult to analyze the dynamics of converter-based FACTS and CP devices, since they incorporate both continuous time dynamics and discrete time events. These analytical difficulties are common in all converter-based components whose operation is based on a switching process. For this reasons, fundamental frequency models are commonly used [Srivastava and Srivastava 1998] [Mithulananthan, et al. 2003].

Since the network between switching instants is nonlinear due to the nonlinear elements in the network, it is not easy to represent the FACTS and CP mathematical models through discrete-time iterative mapping approach. For this reason, accurate mathematical models are needed to carry-out the stability analysis based on the bifurcation theory using a continuation scheme to trace the stability boundaries. The bifurcation analysis based on

continuation schemes allows us to identify not only the stability boundaries but the type of dynamics in each region, as well as the type of bifurcation that emerges in the system.

1.4 Objectives

This investigation is centered on the following main objectives:

1. Efficient modeling of FACTS and Custom Power devices including the harmonic distortion.
2. Development of efficiency methods to compute the periodic steady-state solution of nonlinear components and systems represented by non-autonomous ordinary differential equations.
3. Stability analysis based on bifurcation theory and continuation methods of Custom Power devices. In this analysis, the power system is modeled as instantaneous rather phasor quantities, and the harmonic distortion is taken into account.

1.5 Methodology

In general terms, the construction of a bifurcation diagram consists of the following steps: a) finding a first periodic steady-state solution of ordinary differential equations system, b) based on the first solution, find other equilibrium solutions based on a continuation scheme, and c) determining the stability of each solution.

The results obtained through bifurcation analysis can be shown in a bifurcation diagram, which provides qualitative information about the behavior of the steady state solutions. At certain points (bifurcation points) infinitesimal changes in system parameters can cause significant qualitative changes in periodic solutions.

A continuation algorithm can trace the path of an already established solution, as the parameters are varied. In this thesis, the sequential method [Nayfeh and Balachandran 1995] is used as the predictor; in this method, the periodic solution determined in the previous step is used as an initial guess for the periodic solution to be determined in the next step. The Newton method based on a Discrete Exponential Expansion (DEE) [Segundo-Ramírez and Medina 2009] process is used as the corrector.

The stability of a periodic solution is computed from its Floquet multipliers; they describe the stability around the limit cycle of interest. Floquet theory is based on the fact that a periodic solution can be represented through a fixed-point of an associated Poincaré map [Parker and Chua 1989] [Nayfeh and Balachandran 1995]. Consequently, the stability of a periodic solution can be determined by computing the stability of the corresponding fixed-point of the Poincaré map. The Floquet multipliers are the eigenvalues of the Jacobian of this Poincaré map. Stable periodic solutions correspond to Floquet multipliers inside the unit circle; on the other hand, unstable periodic solutions have at least one characteristic multiplier outside the unit circle. Therefore, loss of stability is encountered when a multiplier leaves the unit circle.

1.6 Contributions

The most significant contributions of this research work are summarized below:

1. An algorithm which dramatically reduces the computer effort required for the identification process of the transition matrix used for the fast steady state solution in the time domain on nonlinear power systems by extrapolation to the limit cycle is introduced. It is demonstrated that the proposed Enhanced Numerical Differentiation (END) Newton method increases the computer efficiency in nearly hundred percent, when compared against the original Numerical Differentiation (ND) method [Semlyen and Medina 1995].
2. A Newton method to compute the periodic steady-state solution of nonautonomous ODE set based on a Discrete Exponential Expansion DEE method. This contribution introduces an efficient methodology for the fast periodic steady state solution of nonlinear power networks. It is based on the application of the Poincaré map to extrapolate the solution to the limit cycle through a Newton method based on a DEE procedure.
3. Two Voltage Source Converters models based on Fourier series and hyperbolic tangent function are proposed. The proposed models can be used for fast simulation in the time domain of power electronic devices based on SPWM VSCs; the undesirable error introduced by the high rates in the commutation instants are removed; even though the harmonic distortion coming from the converter is taken into account. The switching instants in the Fourier model are approximated in a closed form, and an iterative algorithm based on the Newton-Raphson method is developed for the exact calculation of the switching instants. The hyperbolic tangent model does not need the calculation of the switching instants as in the case of the Fourier model.
4. Stability analysis of a DSTATCOM, operating in voltage control mode, using bifurcation theory. The mathematical model of the DSTATCOM in voltage control mode to carry-out the bifurcation analysis is derived. The stability regions in the Thevenin equivalent plane are computed. In addition, the stability regions in the control gains space, as well as the contour lines for different Floquet multipliers are computed. The impact of ac capacitor and dc capacitor on the stability are analyzed through bifurcation theory. The observations are verified through simulation studies. The computation of the stability region allows the assessment the stable operating zones for a power system that includes a DSTATCOM operating in voltage mode.
5. Stability analysis for a DSTATCOM that is operating in current control mode based on bifurcation theory. A control design for the DSTATCOM is proposed. Along with this control, a suitable mathematical representation of the DSTATCOM is proposed to efficiently carry out the bifurcation analysis. The stability regions in the Thevenin equivalent plane are computed for different power factors at the point of common coupling (PCC). In addition, the stability regions in the control gain space,

as well as the contour lines for different Floquet multipliers are computed. The observations are verified through simulation studies.

6. Stability analysis for a DVR connected to an ac system is presented using continuation techniques and bifurcation theory. The system dynamics are explored through the continuation of periodic solutions of the associated dynamic equations. The switching process in the DVR converter is taken into account to trace the stability regions through a suitable mathematical representation of the DVR converter. The stability region in the Thevenin equivalent plane is computed. The bifurcation approach is shown to be both computationally efficient and robust, since it eliminates the need for numerically critical and long lasting transient simulations.

1.7 Thesis Outline

The rest of this thesis is organized into 6 Chapters. A brief overview of each one of these Chapters is given below:

Chapter 2 presents an overview of a collection of controllers which conforms the FACTS and CP technology based on VSCs. Their features, applications, and influences on power systems are briefly described.

Chapter 3 presents the modelling of FACTS and Custom Power devices including harmonic distortion. The proposed models can be used for the efficient computation of the transient and periodic steady state solutions. These models allow the use of a Newton method for efficient computation of the periodic steady state solution. In addition, a larger integration step can be used.

Chapter 4 describes the details of the development of Newton methods based on an Enhanced Numerical Differentiation method (END) and Discrete Exponential Expansion (DEE) procedures, respectively, for the fast and efficient computation of the periodic steady state solution of nonlinear power systems.

Chapter 5 presents the stability analysis for the DSTATCOM operating in voltage control mode, for the DSTATCOM operating in current control mode, and for the DVR.

Chapter 6 draws the overall conclusions of this research and gives suggestions for future research work.

2 A General Overview of Power Converters Employed by FACTS and CP Devices

The STATCOM, SSSC, UPFC, DSTATCOM, DVR, and the UPQC are based on power converters. The power converters employed by FACTS devices have much higher power rating than the custom power devices since they are specially used in bulk power transmission systems [Ghosh and Ledwich 2002]. In addition, the operation principle between the FACTS and CP devices is quite different since it is assumed that the FACTS devices work under balanced sinusoidal conditions, meanwhile, the CP devices have to work under unbalanced, nonsinusoidal and distorted conditions. Consequently, the control strategies and converters structures between the FACTS and CP devices are different. For more details on power electronics please check [Mohan, et al. 1995] and [Rashid 2004].

2.1 Introduction

A power converter is a power electronic circuit that acts as an interface between two different electric systems, for instance, two dc systems with different voltage levels; two electric systems where one is in dc and the other is in ac; or the ac with different frequency. There are two types of ac power converters: Current Source Converter (CSC) and Voltage Source Converter (VSC). The schematic representations of them are shown in Figure 2.1.

A converter has a dc side, a power electronic circuit built of power electronic switches, and an ac side. The power electronic circuit for both CSC and VSC is the same. The ac side is connected to loads or is interfaced to another ac system. Therefore, it is the dc side what differentiates these two converters. The dc input of the CSC is a current source. This current source is usually formed by a controlled dc source that is connected to a large inductor in series. On the other hand, the dc input to a VSC is a dc voltage source that is usually obtained by rectifying an ac voltage, since dc capacitors are more efficient, smaller and less expensive than inductors. Therefore, VSCs are most commonly used in CP and FACTS devices, and we will restrict our discussion to VSCs only.

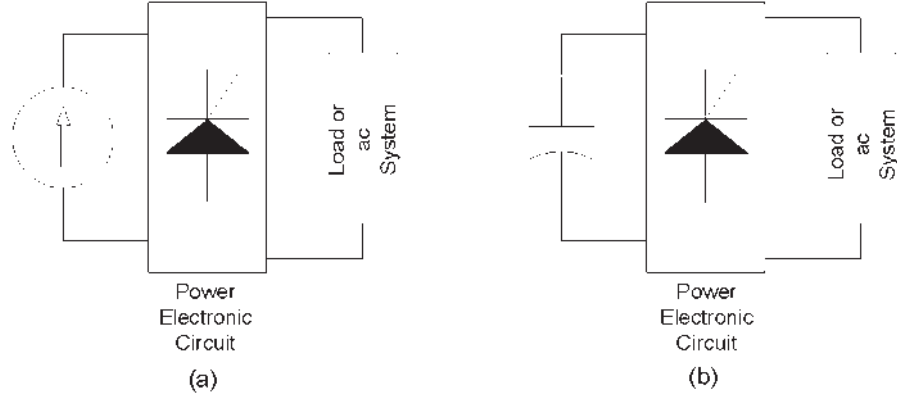


Figure 2.1 Schematic representation of a (a) CSC and (b) VSC

2.2 Inverter Topology

In this section, the structure employed in this investigation will be presented. The state space representation of these topologies will be discussed. In addition, the performance of these inverters is illustrated with the help of some simulation results.

2.2.1 Single-Phase H-bridge Inverter

The schematic diagram of a H-bridge inverter is shown in Figure 2.2. This topology enables a voltage to be applied across the load in either direction. The inverter contains 4 switches S_1 - S_4 , these are power semiconductor devices and anti-parallel diode. The power semiconductor can be a power MOSFET for low power application or a gate turn-off (GTO) thyristor for high power applications. However, for distribution applications, the IGBT is usually used, since it can drive large currents and allows high switching frequencies with low losses.

In Figure 2.2, it is assumed that the load is a RL branch. The load is connected between the two legs of the inverter. The inverter is supplied from a dc voltage, v_{dc} . The switches of each leg have complementary values, e.g. when S_1 is on, S_4 is off and vice versa. In addition, the switches operate in pairs, e.g. when S_1 is on, S_2 is on, and S_3 and S_4 are off, and vice-versa. There is a small time delay provided between the switching on and off of the pairs of semiconductors; this time is called blanking period, and it is provided to prevent the dc source from being short-circuited. For example, in the blanking period, the switch S_1 is getting turned on before S_4 turns off completely. In practice, the blanking time has to be taken into account; however, this period can be neglected for analysis purposes.

In Figure 2.3 the equivalent circuits are presented for the two modes of operation of the H-bridge shown in Figure 2.2. The load current, i_l , is given by

$$\frac{di_l}{dt} = -\frac{R}{L}i_l + \frac{1}{L}v_{dc}u \quad (2.1)$$

where u is defined as

$$u = \begin{cases} 1 & \text{when } S_1 \text{ and } S_2 \text{ are on} \\ -1 & \text{when } S_3 \text{ and } S_4 \text{ are on} \end{cases} \quad (2.2)$$

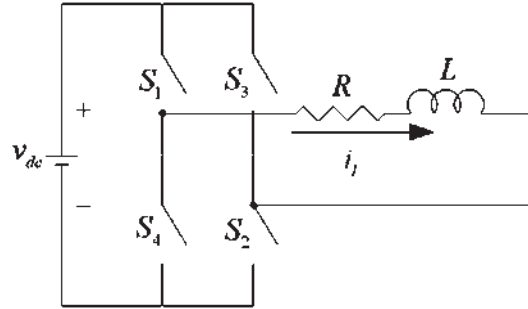
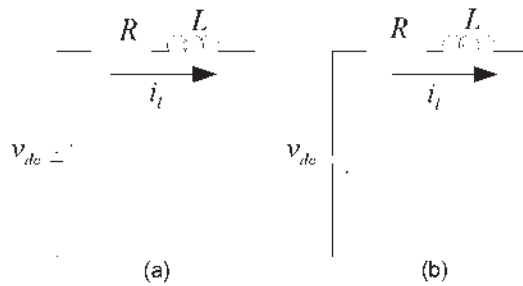


Figure 2.2 Schematic diagram of a H-bridge inverter

Figure 2.3 Equivalent circuits of the H-bridge inverter (a) when S_1 and S_2 are on, and (b) when S_3 and S_4 are on.

Example 2.1: Assuming that

$$v_{dc}=5 \text{ V}, R=1 \Omega, L=2 \text{ mH}, h=0.4 \text{ A}$$

show the operation of the H-bridge through numerical simulations. Let us assume that the tracking reference current (desired current) is given by

$$i_{lref} = \sin \omega t + 0.2 \sin 5\omega t + 0.1 \sin 7\omega t \quad (2.3)$$

where $\omega=120\pi$.

The load reference current, i_{lref} is shown in Figure 2.4. In addition, the hysteresis band is shown between the region $i_{lref}+h$ and $i_{lref}-h$ by mean of the dash line.

The switching function u is computed using the following logic

$$\begin{aligned} & \text{if } i_l - i_{lref} > h \\ & \quad u = -1; \\ & \text{elseif } i_l - i_{lref} < -h \\ & \quad u = 1; \\ & \text{end} \end{aligned} \quad (2.4)$$

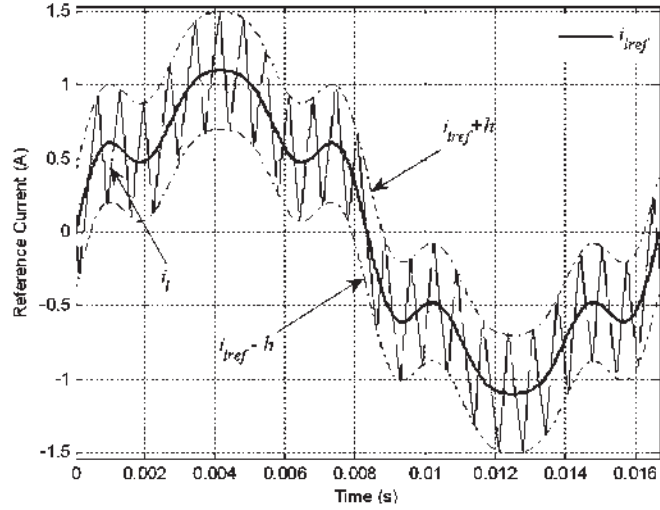


Figure 2.4 Reference current and hysteresis band

In Figure 2.5 the load current is shown for different load inductances. For $L=2$ mH, $L=5$ mH, $L=8$ mH, and $L=11$ mH, in Figure 2.5(a), Figure 2.5(b), Figure 2.5(c), and Figure 2.5(d), respectively. The tracking error, defined as $i_l - i_{lref}$, is shown in Figure 2.6.

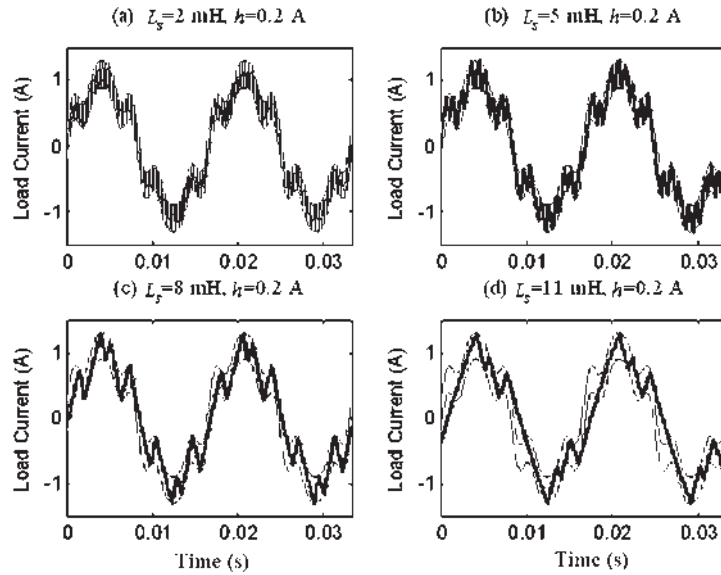


Figure 2.5 Load current for various load inductors

We could conclude from Figure 2.5 that the fundamental frequency of each waveform is 60 Hz since the fundamental frequency of the reference current is 60 Hz; however, this is not the case for each set of parameter values of the circuit shown in Figure 2.2. Figure 2.7 shows a bifurcation diagram computed through the Brute Force (BF) [Parker and Chua 1989] approach to illustrate the performance of the single H-bridge when the load inductor is varied between 2 mH and 162 mH, and $h=0.8$ A. Notice that many periodic steady state

solutions appear when the load inductor is varied. This bifurcation diagram shows that the load current goes out of the hysteresis band for $L > 14.2$ mH.

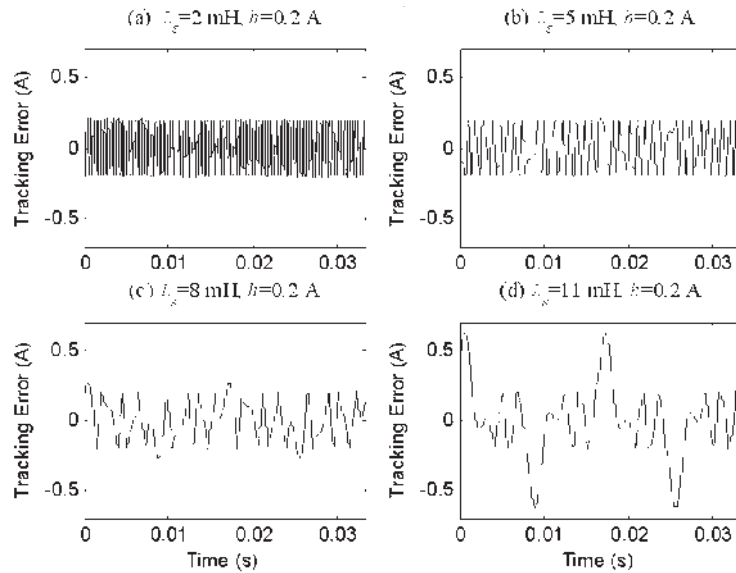


Figure 2.6 Tracking error for various load inductors

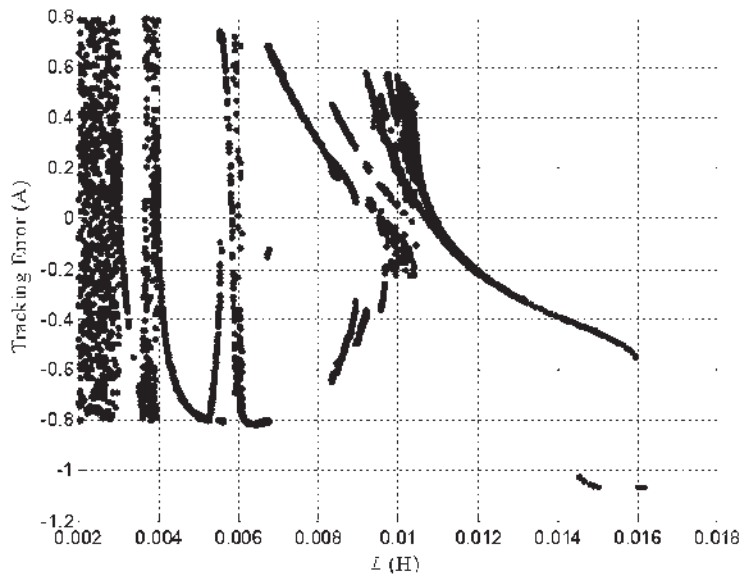


Figure 2.7 Bifurcation diagram of the single H-bridge inverter for $h=0.8$ A

The phase portrait of $i_{ref} - i_l$ for $L=2.2$ mH, and $L=2.38$ mH are shown on Figure 2.8(a) and 2.8(b), respectively. The solution in Figure 2.8(a) is T -periodic, meanwhile in Figure 2.8(b) is $34T$ -periodic.

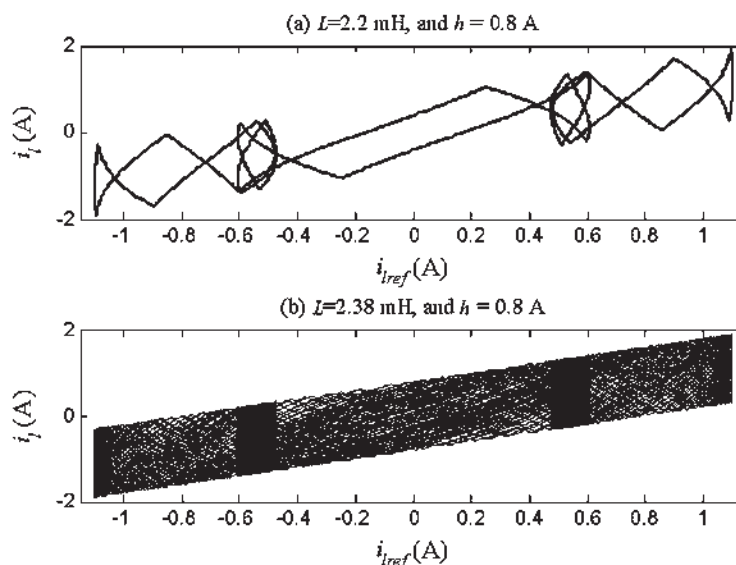


Figure 2.8 Phase portrait of $i_{ref} - i_l$ for (a) $L=2.2$ mH showing a T -periodic solution and for (b) $L=2.28$ mH showing a $34T$ -periodic solution.

For the particular case of the solution shown in Figure 2.8(b), if we use a window of $1/60$ s to carry-out the DFT, there will be interharmonics and subharmonics from the frequency of 60 Hz. However, every component in its spectrum is an integer multiple of the frequency $60/34$ Hz, which is now the fundamental frequency of the $34T$ -periodic steady state solution. Figure 2.9 shows the harmonic spectrum of the periodic steady state solution given in Figure 2.8(b). Observe that the harmonic spectrum contains interharmonics and subharmonics.

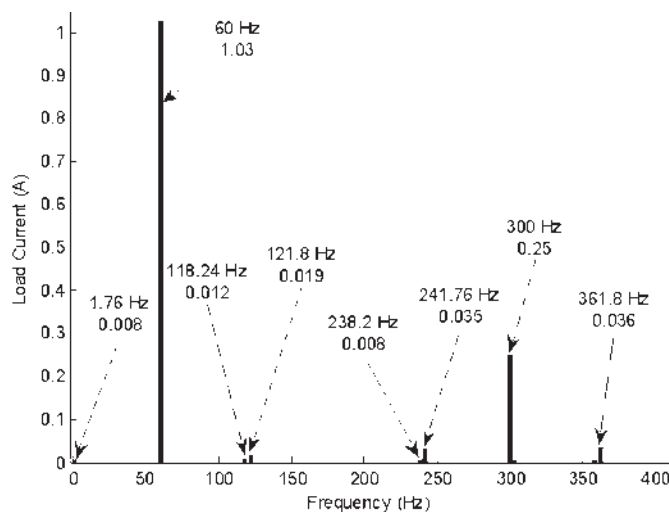


Figure 2.9 Spectrum of the load current

Figure 2.10 shows the bifurcation diagram for $h=0.2$ A. This is different in comparison with that shown in Figure 2.7; however, it still contains several types of periodic solutions. Please observe that the tracking error is within the limits up to $L=5$ mH.

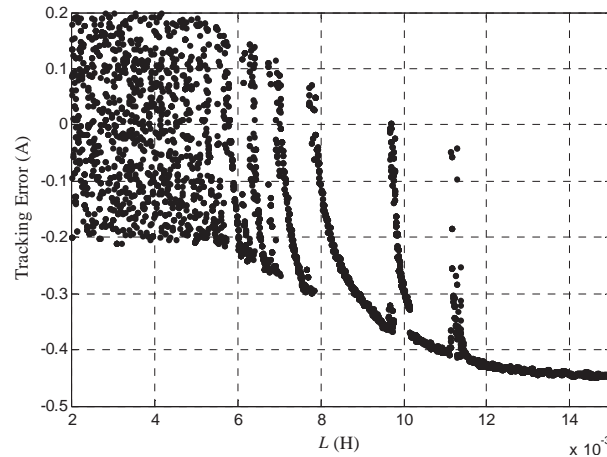


Figure 2.10 Bifurcation diagram of the single H-bridge inverter for $h=0.2$ A

Figure 2.11 shows the periodic steady state solution for different values of the load inductor, e.g. for $L=1.05$ mH in Figure 2.11(a); for $L=1.06$ mH in Figure 2.11(c); and for $L=3.83$ mH in Figure 2.11(e). Please, notice that each solution follows the reference current within the limits imposed by the hysteresis band and apparently the fundamental frequency of each of those solutions is 60 Hz. In order to evaluate the fundamental frequency, the load current has been plotted in discrete times multiples of T , where $T=1/60$ s. In Figure 2.11(b) the solutions are $2T$ -periodic for $L=1.05$ mH; in Figure 2.11(d) the solutions are $5T$ -periodic for $L=1.06$ mH; and in Figure 2.11(f) the solutions are $17T$ -periodic for $L=3.83$ mH.

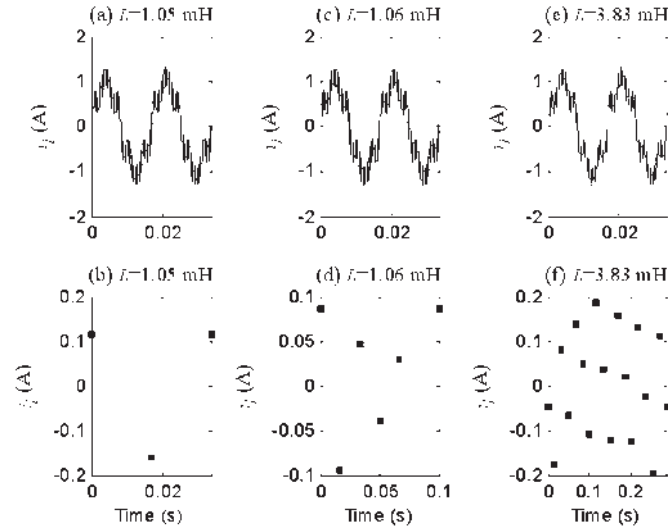


Figure 2.11 Periodic solutions for different load inductors

From these results the following conclusion can be drawn:

- The tracking becomes better as the hysteresis band becomes narrower
- The switching frequency becomes higher as the hysteresis band becomes narrower; however, high switching frequency results in increased losses in the semiconductor switches. Thus, the choice of the hysteresis band is a compromise between tracking error and inverter losses.

- For the same hysteresis band, the switching frequency becomes higher as the load inductor becomes smaller. In addition, the tracking becomes inferior for large load inductors.
- For a large load inductor, even by decreasing the hysteresis band, the tracking is not acceptable since di/dt slowly varies. For a large load inductor, di/dt can be increased by increasing the dc voltage.

2.2.2 Three-Phase H-bridge Inverter

The schematic diagram of a three-phase H-bridge inverter commonly employed in compensating CP devices is shown in Figure 2.12 [Ghosh and Ledwich 2002]. In a practical case, the converter must be able to inject distorted currents in one phase, independently of the other two phases. The three-phase H-bridge inverter is constituted of three single-phase H-bridge inverters connected to a common dc storage capacitor, as shown in Figure 2.12. Each inverter is connected to the load through a transformer. The transformers are used to provide isolation between the inverter legs. This also prevents the dc capacitor from short circuits between phases. The compensating devices based on this structure can independently compensate each phase. It is to be noticed that due to the presence of transformers, this topology is not suitable for cancelling-out any dc component in the load current. The inductance L_f represents the leakage inductance of each transformer and the additional external inductance, if any. The switching losses of an inverter and the copper loss of the connecting transformer are represented by a resistance R_f .

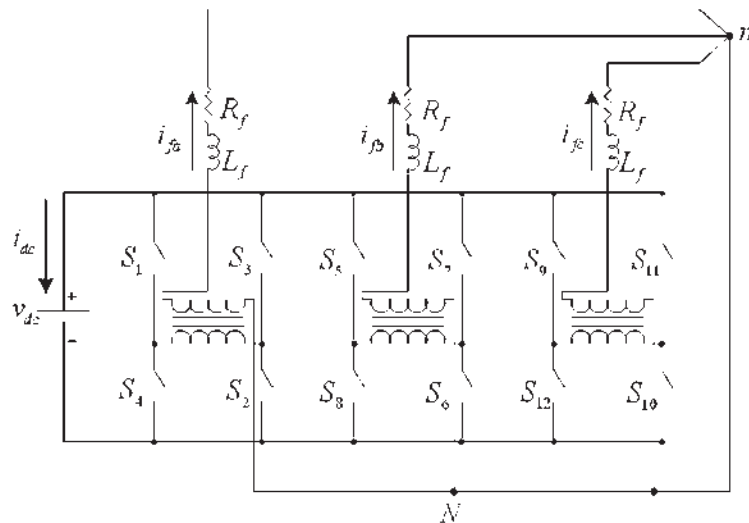


Figure 2.12 Schematic diagram of a three-phase H-bridge inverter

The switches of each leg have complementary values, e.g. when S_1 is on, S_4 is off and vice versa. Additionally, the switches are operated in pairs, when S_1 is on, and S_2 is on, S_3 and S_4 are off, and vice versa.

The load currents, i_f , are given by

$$\begin{aligned}
\frac{di_{fa}}{dt} &= -\frac{R_f}{L_f}i_{fa} + \frac{1}{L_f}v_{dc}u_a \\
\frac{di_{fb}}{dt} &= -\frac{R_f}{L_f}i_{fb} + \frac{1}{L_f}v_{dc}u_b \\
\frac{di_{fc}}{dt} &= -\frac{R_f}{L_f}i_{fc} + \frac{1}{L_f}v_{dc}u_c
\end{aligned} \tag{2.5}$$

where

$$\begin{aligned}
u_a &= \begin{cases} 1 & \text{when } S_1 \text{ and } S_2 \text{ are on} \\ -1 & \text{when } S_3 \text{ and } S_4 \text{ are on} \end{cases} \\
u_b &= \begin{cases} 1 & \text{when } S_5 \text{ and } S_6 \text{ are on} \\ -1 & \text{when } S_7 \text{ and } S_8 \text{ are on} \end{cases} \\
u_c &= \begin{cases} 1 & \text{when } S_9 \text{ and } S_{10} \text{ are on} \\ -1 & \text{when } S_{11} \text{ and } S_{12} \text{ are on} \end{cases}
\end{aligned} \tag{2.6}$$

The dc current is given by

$$i_{dc} = -(i_{fa}u_a + i_{fb}u_b + i_{fc}u_c) \tag{2.7}$$

Example 2.2 Generate the following currents

$$\begin{aligned}
i_{fa}^{ref} &= 1.3 \sin \omega t + 0.2 \sin 5\omega t + 0.1 \sin 7\omega t \\
i_{fb}^{ref} &= \sin(\omega t - 2\pi/3) + 0.1 \sin 5(\omega t - 2\pi/3) + 0.3 \sin 7(\omega t - 2\pi/3) \\
i_{fc}^{ref} &= 1.1 \sin(\omega t + 2\pi/3) + 0.15 \sin 5(\omega t + 2\pi/3) + 0.2 \sin 7(\omega t + 2\pi/3)
\end{aligned} \tag{2.8}$$

Assuming that

$$v_{dc}=5 \text{ V}, R=1 \text{ } \Omega, L=2 \text{ mH}, h=0.1 \text{ A and } \omega=120\pi$$

The current tracking results are shown in Figure 2.13(a), and the neutral current is shown in Figure 2.13(b). Notice that the error in the neutral current is higher than the error in the phase currents since this is the sum of errors in the three currents.

In Figure 2.14 the bifurcation diagram using L_f as a bifurcation parameter is shown. The operation of the converter when the tracking error is within the limits ($L_f < 5\text{mH}$) imposed by the hysteresis band introduces harmonics, subharmonics, and interharmonics, since its solution is not T -periodic.

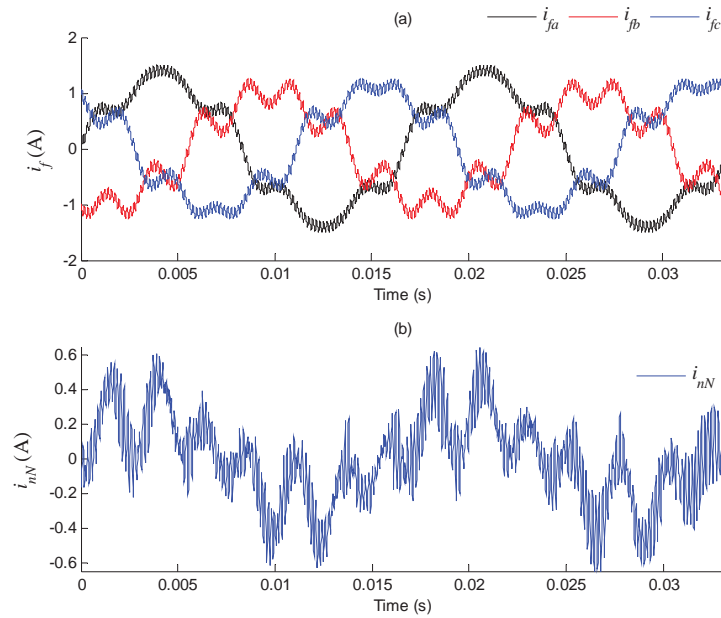


Figure 2.13 Currents for the three-phase H-bridge inverter (a) load currents, and (b) neutral current

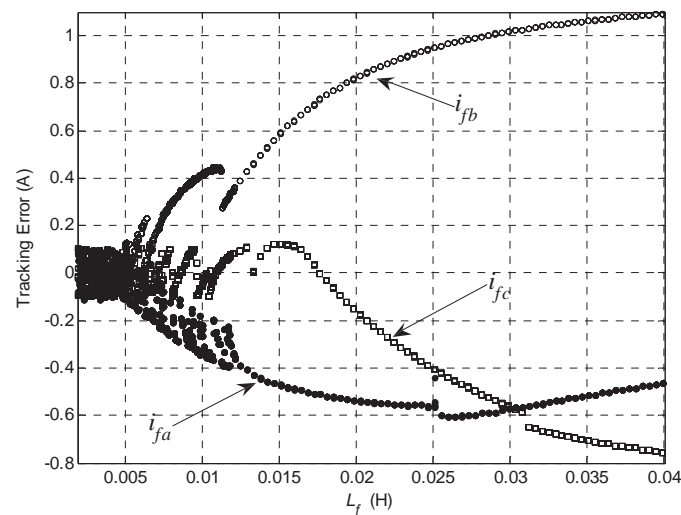


Figure 2.14 Bifurcation diagram for the three-phase H-bridge inverter

2.2.3 Three-Phase Inverter

A schematic diagram of a three-phase inverter is shown in Figure 2.15. It consists of six semiconductor switches S_1 - S_6 . In this configuration, the switches of each leg are complementary, it means that when one switch is on the other is off. For example, when S_1 is on, S_4 is off and vice versa. The inverter is supplied by two equal dc sources $v_{dc}/2$. The load neutral is denoted by n , meanwhile the converter neutral is denoted by N .

In order to show the modeling of this inverter, we have assumed for simplicity a RL load ($R_f + j\omega L_f$). However, this analysis can be applied for any different load. For inspection, the voltage across the point a and the converter neutral is

$$v_{aN} = \begin{cases} \frac{v_{dc}}{2} & \text{if } S_1 \text{ is on} \\ -\frac{v_{dc}}{2} & \text{if } S_4 \text{ is on} \end{cases} \quad (2.9)$$

Similar equation can be obtained for v_{bN} , and v_{cN} .

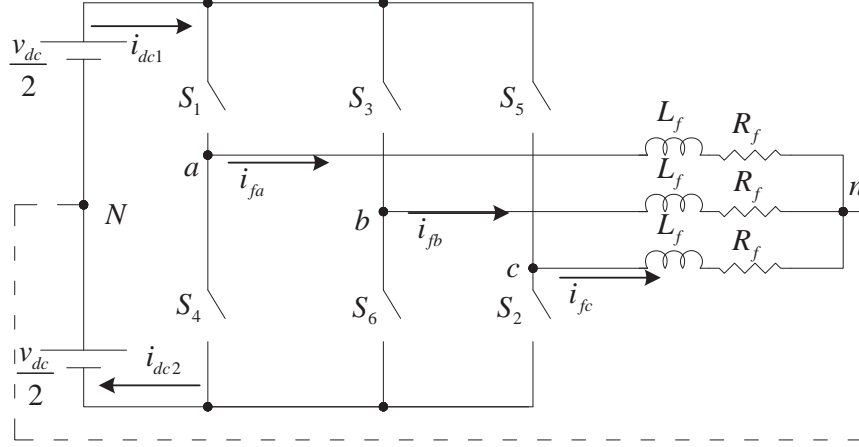


Figure 2.15 Schematic diagram of a three-phase inverter

Assuming that the path Nn is open, the voltage between n and N , v_{nN} , is non zero. Thus, the state equation can be written as

$$L_f \frac{di_{fa}}{dt} = -R_f i_{fa} + \frac{v_{dc}}{2} u_a - v_{nN} \quad (2.10a)$$

$$L_f \frac{di_{fb}}{dt} = -R_f i_{fb} + \frac{v_{dc}}{2} u_b - v_{nN} \quad (2.10b)$$

$$L_f \frac{di_{fc}}{dt} = -R_f i_{fc} + \frac{v_{dc}}{2} u_c - v_{nN} \quad (2.10c)$$

u_a , u_b , and u_c are the switching functions defined as

$$u_a = \begin{cases} +1 & \text{if } S_1 \text{ is on} \\ -1 & \text{if } S_4 \text{ is on} \end{cases} \\ u_b = \begin{cases} +1 & \text{if } S_3 \text{ is on} \\ -1 & \text{if } S_6 \text{ is on} \end{cases} \\ u_c = \begin{cases} +1 & \text{if } S_5 \text{ is on} \\ -1 & \text{if } S_2 \text{ is on} \end{cases} \quad (2.11)$$

The system is a three-phase, three-wire configuration, and the load neutral point is floating, therefore

$$i_{fa} + i_{fb} + i_{fc} = 0 \quad (2.12)$$

Because of (2.12) has to be satisfied, the three-phase, three-wire configuration is not suitable for independently tracking the three currents.

The voltage between n and N can be obtained from (2.10) and (2.12), and can be written as

$$v_{nN} = \frac{v_{dc}}{6}(u_a + u_b + u_c) \quad (2.13)$$

The dc currents i_{dc1} and i_{dc2} are given by,

$$\begin{aligned} i_{dc1} &= i_a S_1 + i_b S_3 + i_c S_5 \\ i_{dc2} &= i_a S_4 + i_b S_6 + i_c S_2 \end{aligned} \quad (2.14)$$

Remember that S_i is 0 when open, and 1 when closed, with $i=1,2,\dots,6$.

If the two neutral points are connected, $i_{dc1} = i_{dc2}$, and the restriction (2.12) can no longer be imposed, then

$$v_{nN} = 0 \quad (2.15)$$

Example 2.3 Generate the following currents

$$\begin{aligned} i_{fa}^{ref} &= I_a (\sin \omega t + 0.2 \sin 5\omega t + 0.1 \sin 7\omega t) \\ i_{fb}^{ref} &= I_b (\sin(\omega t - 2\pi/3) + 0.2 \sin 5(\omega t - 2\pi/3) + 0.1 \sin 7(\omega t - 2\pi/3)) \\ i_{fc}^{ref} &= I_c (\sin(\omega t + 2\pi/3) + 0.2 \sin 5(\omega t + 2\pi/3) + 0.1 \sin 7(\omega t + 2\pi/3)) \end{aligned} \quad (2.16)$$

Assuming that

$$v_{dc}=5 \text{ V}, R=1 \text{ } \Omega, L=2 \text{ mH}, h=0.05 \text{ A}, \text{ and } \omega=120\pi$$

Case 1: Balanced reference current

In the balanced case

$$I_a = I_b = I_c = 1 \text{ A} \quad (2.17)$$

The load currents are shown in Figure 2.16(a), and the neutral current is shown in Figure 2.16(b). Please observe that the neutral current is not zero even for a balanced load and reference current, in spite of the reference current does not have any triplen harmonic. However, the load currents contain triplen harmonics. This current is due to the switching process.

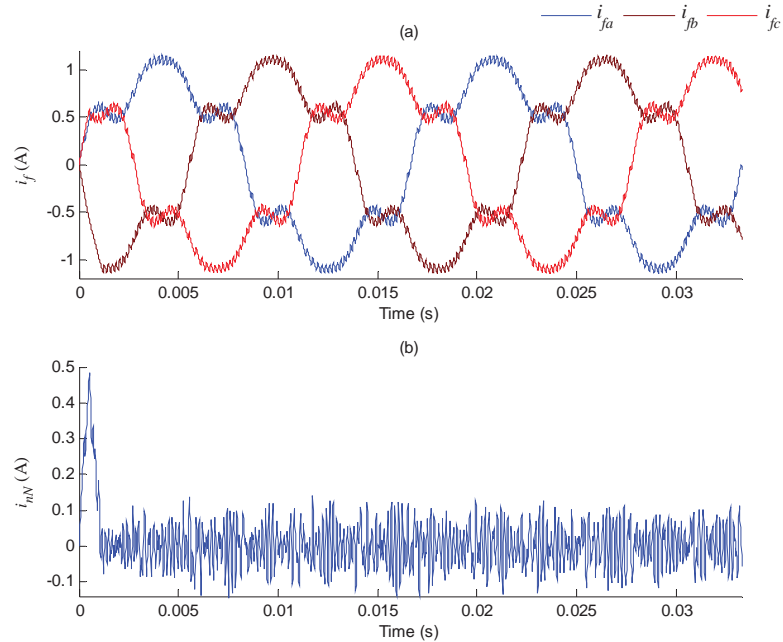


Figure 2.16 Currents for the three-phase inverter (a) load currents, and (b) neutral current

The bifurcation diagram for the three-phase converter is shown in Figure 2.17. Notice that the tracking error is maintained within the limits up to $L_f < 3.5$ mH. In addition for $L_f < 3.5$ mH the converter has several types of solutions. For instance, for $L_f = 2$ mH the solution has period 7, and for $L_f = 3.29$ mH the periodic solution has period T (1/60 s); these can be seen in Figure 2.18(a) and Figure 2.18 (b), respectively. In this Figure, i_{fa} is plotted in discrete time multiples of T .

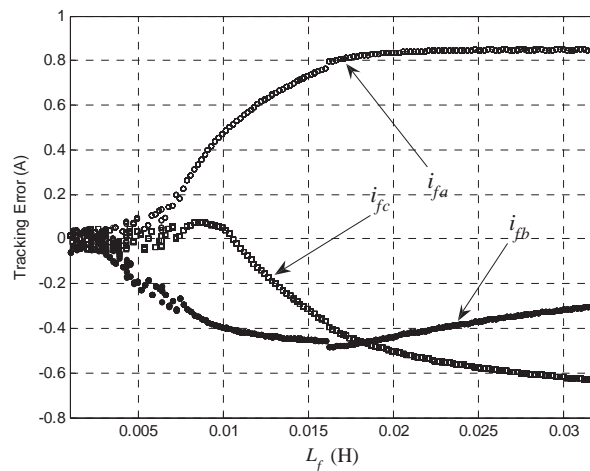


Figure 2.17 Bifurcation diagram for the three-phase inverter: balanced case

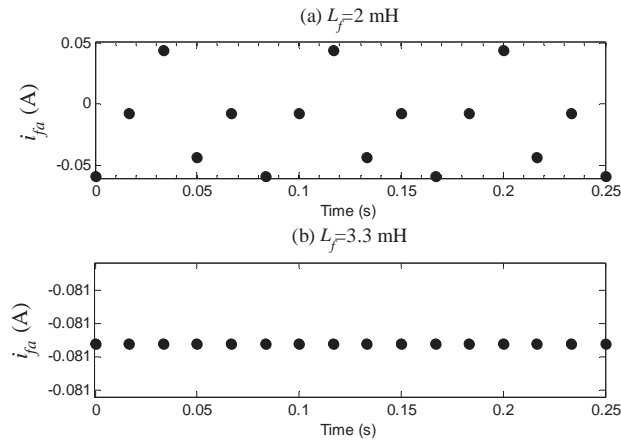


Figure 2.18 Periodic solution for different load inductors (a) $L_f=2$ mH, and (b) $L_f=3.3$ mH

Case 2: Unbalanced reference current

In this case

$$I_a = 0.8 \text{ A}, I_b = 1.5 \text{ A}, \text{ and } I_c = 1.1 \text{ A} \quad (2.18)$$

The current tracking results are shown in Figure 2.19. Notice that the neutral current is significantly higher, when compared with the balanced case. The error in the neutral current is higher than the tracking error in the load currents since the hysteresis modulation scheme controls only the error in the load current but it does not directly control the error in the neutral current.

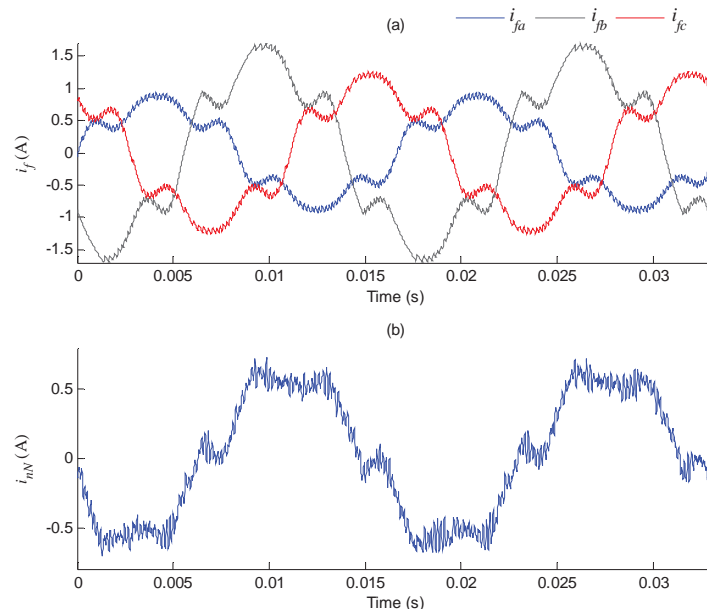


Figure 2.19 Currents for the three-phase inverter (a) load currents, and (b) neutral current

Figure 2.20 shows the bifurcation diagram of the three phase converter for the unbalanced case. In this case, there are also several types of periodic steady-state solutions. Notice also that the tracking error cannot be within the limits for $L_f > 2.5$ mH.

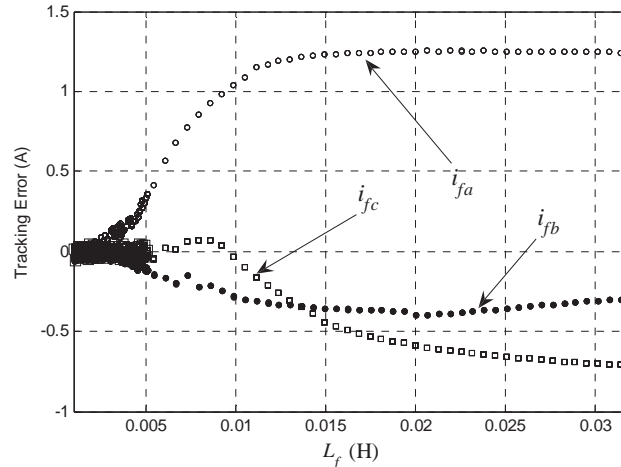


Figure 2.20 Bifurcation diagram for the three-phase inverter: unbalanced case

2.2.4 Six-Pulse Voltage Source Converter

The circuit representation of a six-pulse converter is shown in Figure 2.21. The bidirectional switching function is identified by S_i and S'_i for each phase ($i=a,b,c$), which can be on or off, r is the switch-on state resistance, S_i is 1 or 0, corresponding to the on and off states of the switch, respectively. In addition, S_i and S'_i are complementary, e.g. $S_i + S'_i = 1$.

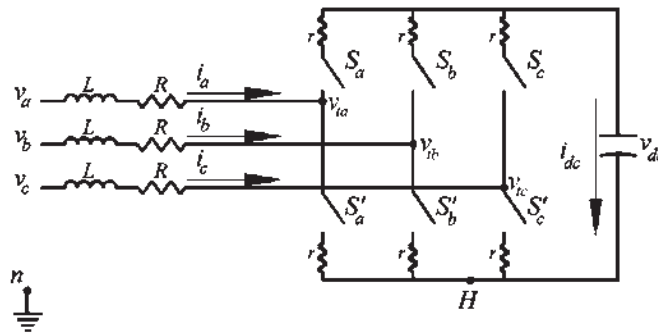


Figure 2.21 Three-phase Six-pulse converter

To describe the mathematical model of this converter, let us consider the phase A and the dc side as shown in Figure 2.22.

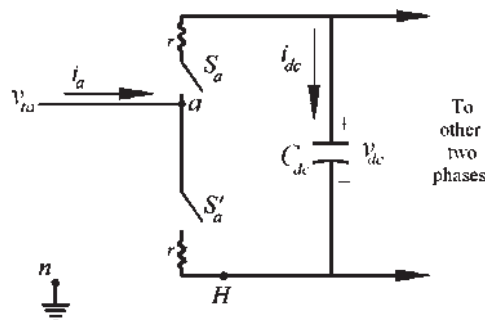


Figure 2.22 Equivalent circuit of phase A

The equation that describes the voltage v_{ta} can be written as

$$v_{ta} = v_{aH} + v_{Hn} \quad (2.19)$$

When S_a is on we have

$$v_{aH} = (ri_a + v_{dc})S_a \quad (2.20)$$

On the other hand, when S_a is off we have

$$v_{aH} = ri_a S'_a \quad (2.21)$$

Since S_a and S'_a are complementary

$$v_{aH} = ri_a + v_{dc}S_a \quad (2.22)$$

Similar equations are found for the other two phases:

$$v_{bH} = ri_b + v_{dc}S_b \quad (2.23)$$

$$v_{cH} = ri_c + v_{dc}S_c$$

Since $v_{ta} + v_{tb} + v_{tc} = 0$ and $i_a + i_b + i_c = 0$, we obtain

$$v_{Hn} = -\frac{v_{dc}}{3}(S_a + S_b + S_c) \quad (2.24)$$

Then, the terminal voltage can be expressed as

$$v_{ta} = ri_a + v_{dc}S_a - v_{dc}/3(S_a + S_b + S_c)$$

$$v_{tb} = ri_b + v_{dc}S_b - v_{dc}/3(S_a + S_b + S_c) \quad (2.25)$$

$$v_{tc} = ri_c + v_{dc}S_c - v_{dc}/3(S_a + S_b + S_c)$$

Equations (2.25) can be represented by the circuit of Figure 2.21; however, an alternative equivalent circuit for (2.25) is shown in Figure 2.23.

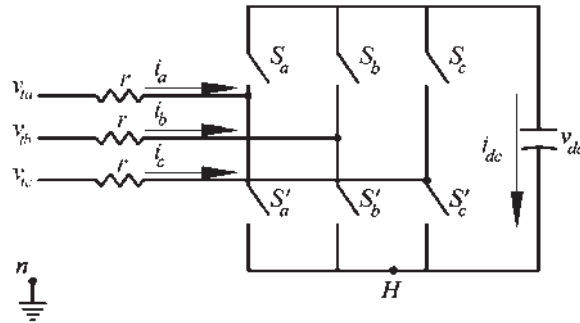


Figure 2.23 Equivalent three-phase six-pulse converter model

The dynamics of the dc capacitor, C_{dc} , is

$$\frac{dv_{dc}}{dt} = \frac{1}{C_{dc}} i_{dc} \quad (2.26)$$

The dc current i_{dc} can be obtained using the using the energy preservation principle, e.g.

$$P_{ac} = P_{dc} + P_{loss} \quad (2.27)$$

where

$$P_{ac} = v_{ta} i_a + v_{tb} i_b + v_{tc} i_c \quad (2.28)$$

and

$$P_{dc} = v_{dc} i_{dc} \quad (2.29)$$

p_{loss} is the switching loss and it is expressed as

$$p_{loss} = r(i_a^2 + i_b^2 + i_c^2) \quad (2.30)$$

From (2.28) and (2.29), we can express i_{dc} as

$$i_{dc} = \frac{v_{ta} i_a + v_{tb} i_b + v_{tc} i_c - P_{loss}}{v_{dc}} \quad (2.31)$$

Using (2.25) and (2.30), the dc current can be also expressed as

$$i_{dc} = i_a S_a + i_b S_b + i_c S_c - (i_a + i_b + i_c)(S_a + S_b + S_c) / 3 \quad (2.32a)$$

Since $i_a + i_b + i_c = 0$, i_{dc} takes the form,

$$i_{dc} = i_a S_a + i_b S_b + i_c S_c \quad (2.32b)$$

2.2.5 Sinusoidal Pulse Width Modulation (SPWM)

Consider one arm of a converter as illustrated in Figure 2.22. The desired signal (reference signal) is v_s and the dc voltage across the capacitor is v_{dc} . The reference signal is defined as

$$v_s = E_s \cos(\omega t + \alpha) \quad (2.33)$$

E_s is the magnitude of v_s , and α is its phase angle. The purpose is to transform the continuous v_s into a series of pulses having a fixed amplitude v_{dc} . To achieve this result, a sawtooth wave (*tri*) with a magnitude of v_{dc} is drawn. Now, conduction takes place whenever v_s lies above the triangular waveform (*tri*), and conduction ceases whenever it

lies below. The resulting pulse train contains the signal $v_s/2$. The amplitude of the triangular signal is kept constant. The SPWM process is illustrated by Figure 2.24(a). The corresponding switching function is shown in Figure 2.24.

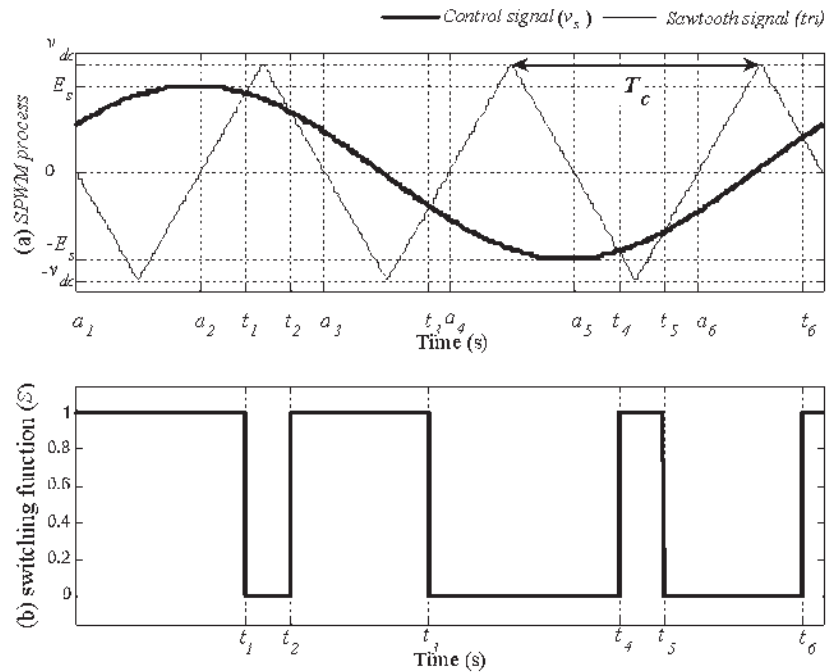


Figure 2.24 Transforming a desired continuous signal v_s into a SPWM signal.

In practice, T_c is much shorter than that shown in Figure 2.24. Consequently, the change in v_s during one carrier period T_c is considerably less than the indicated in Figure 2.24(a). In other words, a higher carrier frequency f_c directly improves the reproduction of the original signal v_s ; the carrier frequency f_c is defined as $1/T_c$.

The frequency-modulation ratio m_f is defined as f_c/f_s , where f_s is the frequency of v_s . Higher m_f implies a high switching frequency.

The SPWM technique can be also applied to the converter structure illustrated in Figure 2.15.

Example 2.4 For the circuit shown in Figure 2.25, find the fundamental terminal voltage for different amplitude modulation ratios and for different frequency modulation ratios. Assume $v_{dc}=10$ V.

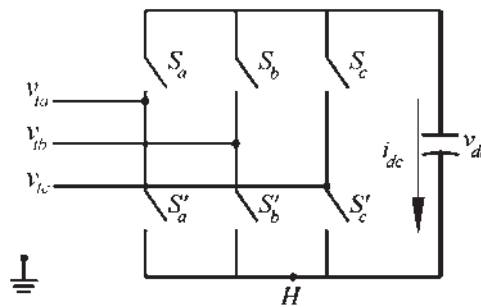


Figure 2.25 Circuit of example 2.4

In Figure 2.26 the magnitude of the fundamental terminal voltage, in terms of the dc voltage capacitor for different frequency modulation ratios (m_a) is shown; Figure 2.27 shows nonlinear range for magnitude of the fundamental frequency voltage control by varying m_a , where m_a is defined as E_s/v_{dc} .

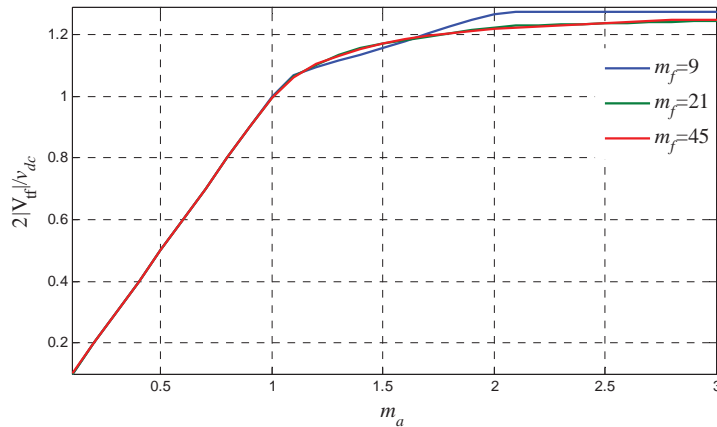


Figure 2.26 Voltage control by varying m_a

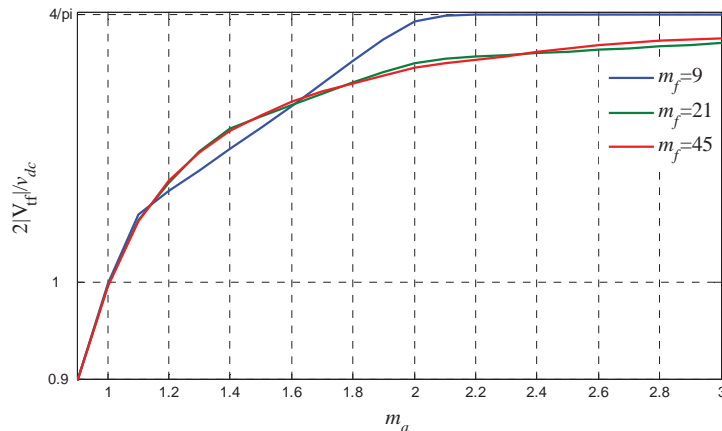


Figure 2.27 Nonlinear range for magnitude of the fundamental frequency voltage control by varying m_a

Observe that for $m_a \leq 1$, the terminal voltage is directly proportional to m_a in spite of the frequency modulation ratio. However, this relation becomes nonlinear for $m_a > 1$. Thus, since the amplitude of the fundamental frequency terminal voltage varies linearly with m_a for $m_a \leq 1$, this range is called linear modulation; meanwhile, for $m_a > 1$ results in what is called overmodulation [Mohan, et al. 1995]. In the overmodulation ratio, the relation between the dc voltage capacitor and the terminal voltage depends on the used frequency modulation ratio.

In the linear modulation, the SPWM pushes around the switching frequency and its multiples. One of the main drawbacks is that the maximum available amplitude of the fundamental frequency component is not as high as we would wish. To increase the amplitude of the fundamental frequency component in the terminal voltage, the index amplitude modulation, m_a , is increased beyond $m_a=1$. However, overmodulation causes the

output voltage to contain many more harmonics in the sidebands, as compared with the linear modulation.

In Figure 2.28(a) the terminal voltage and its fundamental frequency component are shown for $m_a = 0.8$ and $m_f = 15$. On the other hand, in Figure 2.28(b) the harmonic spectrum of v_{ta} in terms of $v_{dc}/2$ is illustrated. Please observe that for $m_a \leq 1$, the fundamental frequency component of v_{ta} is m_a times $v_{dc}/2$. Choosing m_f as an odd integer results in odd symmetry as well as a half-wave symmetry with the origin. For more details on SPWM please review [Mohan, et al. 1995].

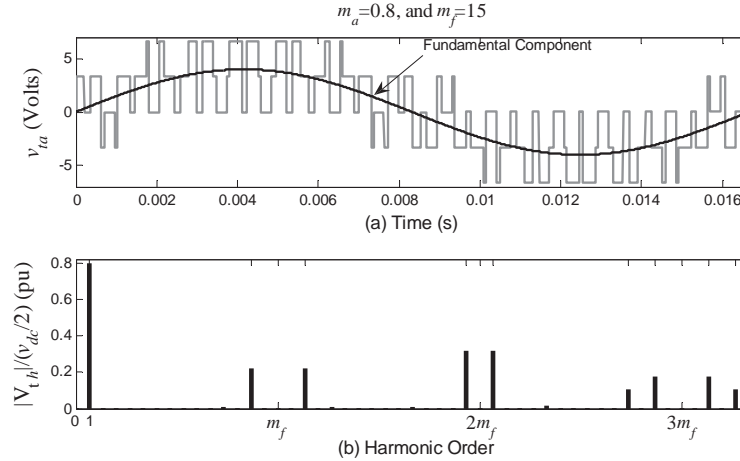


Figure 2.28 Sinusoidal pulse width modulation (a) voltage at the terminal of the converter. (b) Harmonic spectrum of the voltage at the terminal of the converter in terms of the dc voltage capacitor

2.3 Simplified Models

2.3.1 Fundamental Frequency Component of the Switching Functions for the SPWM

Fundamental component of the switching function obtained with the SPWM technique for the converter topologies shown in Figure 2.15 and Figure 2.21 are

$$\begin{aligned}
 S_a &= 0.5 + \frac{m_a}{2} \cos(\omega t + \alpha) \\
 S_b &= 0.5 + \frac{m_a}{2} \cos(\omega t + \alpha - 2\pi/3) \\
 S_c &= 0.5 + \frac{m_a}{2} \cos(\omega t + \alpha + 2\pi/3)
 \end{aligned} \tag{2.34}$$

Using (2.34), the fundamental frequency voltage at the terminals of the converter can be expressed as,

$$\begin{aligned}
v_{ia} &= \frac{m_a v_{dc}}{2} \cos(\omega t + \alpha) \\
v_{ib} &= \frac{m_a v_{dc}}{2} \cos(\omega t + \alpha - 2\pi / 3) \\
v_{ic} &= \frac{m_a v_{dc}}{2} \cos(\omega t + \alpha + 2\pi / 3)
\end{aligned} \tag{2.35}$$

Similar equations can be obtained for the converter shown in Figure 2.15. The switching functions u_a , u_b , and u_c used in (2.10) can be represented in terms of S_a , S_b , and S_c as follows

$$\begin{aligned}
u_a &= 2S_a - 1 \\
u_b &= 2S_b - 1 \\
u_c &= 2S_c - 1
\end{aligned} \tag{2.36}$$

Using the fundamental component of the switching functions, the dc currents i_{dc1} and i_{dc2} are equal if the neutrals are connected or not.

2.3.2 Simplified Representation of the Hysteresis Modulation Technique

In the detailed model, the switching devices, the modulation process and the dc capacitor dynamic are explicitly represented. The switching elements are modeled as ideal switches. This model sometimes requires very small times to well represent the commutation process, thus, the simulation time could be considerably long. If we are not interested in the chopping, one can use a source having the average value computed upon a chopping period. With the simplified model, one can simulate the system using a larger time step.

There are two ways for obtaining a simplified representation of the hysteresis modulation technique. The first one is to assume the converter as a set of ideal current or voltage sources. The second one is to assume $h=0$ for the hysteresis band modulation, which we call zero hysteresis band approach.

2.3.2.1 Ideal Sources

For this approach, the converter can be replaced by three ideal current or voltage sources, depending on the case. In this approach it is assumed that the converter is able to instantaneously generate the reference currents or voltages. From this assumption, all the mathematical equations of the power network are developed. The link between the dc side and the ac side is well represented using the energy preservation principle.

2.3.2.2 Smooth Hysteresis Band Approach

In the ideal sources approach we assume an instantaneous response of the converter to generate the reference currents and voltages. However, this approach does not take into account the switching control (LQR, dead-beat, etc.) nor the converter structure. The

smooth-hysteresis band approach is simpler than the ideal sources approach, since it is possible to obtain the simplified model from the detailed model directly. In addition, this approach takes into account the converter structure and the switching control.

This method is based on the next observation: suppose that the hysteresis band is decreased until $h=0$; as a consequence the harmonic distortion introduced by the converter no longer exists.

The hysteresis curve in the detailed model can be replaced for a sigmoid function or a hyperbolic tangent. The sigmoid function is also called the sigmoidal curve or logistic function. The approximation of the hysteresis curve using the sigmoid function is defined as

$$u = \frac{2}{1 + e^{\frac{4u_c}{h}}} - 1$$

The approximation through the hyperbolic tangent is defined as

$$u = -\tan h\left(\frac{u_c}{h}\right)$$

Here, u_c is a continuous function defined as the controlled current or voltage obtained from measurements minus the reference signal. Figure 2.29 shows the hysteresis function represented with solid lines; the smooth hysteresis curve is drawn with dashed lines.

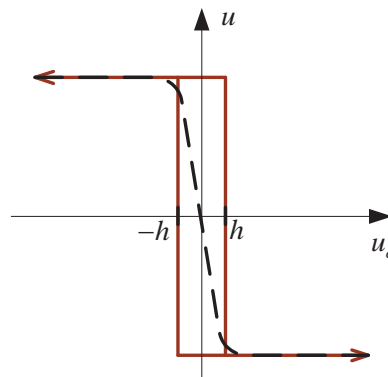


Figure 2.29 Hysteresis modulation technique and the smooth hysteresis approximation

2.4 Conclusions

In this chapter the structures of various converters circuits have presented; these structures are widely used in FACTS and custom power devices. In addition, the sinusoidal pulse width and the hysteresis modulation techniques have been presented, these are used in FACTS and custom power devices, respectively. Several examples have been presented to illustrate the performance of these converters and modulation techniques.

Bifurcation diagrams for the H-bridge and the three-phase 4-wires converters modulated with the hysteresis band technique has been reported, and it has been illustrated that this modulation technique normally works with a period longer than the fundamental one. From

the stability point of view, this modulation technique cause loss of stability as shown in examples 2.1 and 2.2; however, for practical purposes, the instability is retained in the hysteresis band and it can be neglected. The SPWM does not present stability problems.

3 Modeling of FACTS and Custom Power Devices

In this chapter two Voltage Source Converters (VSC) models based on Fourier series and hyperbolic tangent function are proposed. The models are described in detail. The proposed models can be used for fast simulation in the time domain of power electronic devices based on SPWM VSCs. The undesirable error introduced by the high rates in the commutation instants are removed; even though the harmonic distortion coming from the converter is taken into account. The switching instants in the Fourier model are approximated in a closed form, and an iterative algorithm based on the Newton-Raphson method is developed for the exact calculation of the switching instants. The hyperbolic tangent model does not need the calculation of the switching instants as in the case of the Fourier model. These models can be extended to FACTS and custom power devices. In particular these models are directly applied to FACTS devices based on SPWM VSCs. however, for custom power devices is not that easy since the power converters employed in custom power devices usually have different topologies in comparison with FACTS technology [Ghosh and Ledwich 2002]. In general, the converters can be modeled using the energy preservation principle approach to obtain average models. If the converter is modulated in a hysteresis fashion, then the approaches described in Section 2.3.2 can be applied. The proposed models are validated against the solution obtained with the Power System Blockset (PSB) of Simulink and with PSCAD/EMTDC. The VSC model based on Fourier series approach hyperbolic tangent are validated against the response obtained by measurements from a 1.5 kVA ASD experimental setup system.

3.1 Modeling of FACTS Devices Based on SPWM VSCs

The FACTS technology is the application of power electronics in transmission systems [Hingorani and Gyudyi 2000]. The main purpose of this technology is to control and regulate the electric variables in power systems. This is achieved by using converters as a controllable interface between two power system terminals. The resulting converter representation can be useful for a variety of configurations.

Basically, the family of FACTS devices based on Voltage Source Converters (VSCs) consists of a series compensator (SSSC), a shunt compensator (STATCOM), and a shunt/series compensator (UPFC). In Figure 1.1 a schematic representation of the STATCOM, the SSSC, and the UPFC is presented.

To understand and control the interactions between the FACTS devices based on VSCs and the utility system, there is a need for appropriate models to obtain fast and accurate results. There are several models of the FACTS devices based on ideal VSCs; [Uzunovic, et al. 1998], [Nabavi-Niaki and Iravani 1996], [Tavakoli-Bina and Hamill 2005], [Uzunovic, et al. 1997], and [Cañizares 2000]. This approach is frequently used due to its simplicity. However, these models have evident limitations to evaluate the harmonic distortion introduced into the power system by the VSCs, as well as the phenomena related to the switching process in the VSCs.

With any VSC application, converter-based FACTS equipment act as a source of harmonic current injection into the system and it also interacts with harmonic distortions present within the system. The representation of the harmonic interaction between these devices and the network, as well as its impact in the system, can be achieved from an accurate mathematical model of the VSC. This model can give a clear perception about the performance of the FACTS devices, as well as the possibility to determinate the harmonic distortion produced by these devices and to assess its adverse power quality impact. However, it is difficult to analyze the dynamics of voltage source converter systems, since they incorporate both continuous time dynamics and discrete time events. These analytical difficulties are common in all FACTS components since their operations are based on a switching process.

The switching devices employed in these VSC-based FACTS are semiconductor switches. Modeling of switches devices can be performed with different levels of detail. A very detailed model can be justified and necessary when we are interested on studying any phenomena associated with the switching process, but typically the computational cost is very high because the Ordinary Differential Equations (ODEs) that model the electric system become stiff, requiring a stiff ODE solver, since small time-constants are introduced. Besides, the derivatives are very large during the switching transitions, requiring very small values of the integration step to be used, and probably causing the non-convergence of the iterative solver of the implicit ODE method; typically, the Newton-Raphson method. On the other hand, in power systems we are more interested on a fundamental understanding, for this reason in most cases it is advantageous to model the switch as an open and short circuit, respectively. However, this model has some disadvantages; for instance, inconsistent initial conditions can appear [Vlach, et al. 1995]. The source of these numerical problems are the discontinuities and the non-differentiability introduced for the ideal switch; e.g. to numerically follow the trajectory of an ODE system, the solution can be achieved using a sufficiently small integration step if the solution of the system is continuous and smooth. However, this is not satisfied by power electronic devices based on ideal switches models. Please notice that the original continuous ODE system representation of the electric circuit becomes a discontinuous ODE system when we replace the real model of the semiconductor switch by the ideal switch model. An important problem arising from this model is that the numerical error introduced by discontinuities does not allow computing the solution to a very high precision. Conventional numerical integration methods, such as the trapezoidal rule has a marked difficulty to achieve a high precision in power electronic systems. The interpolation techniques incorporated in PSCAD/EMTDC [HVDC Research Centre 2003] have shown to give better results in the simulation of electric circuits including switching events, even allow the use of much larger integration steps. However, the numerical solution cannot be computed to a high precision,

especially when more than one switching event takes place during one integration step. Alternatively, the switching instant can be exactly integrated, then switch and then proceed to integrate the switched system [Hiskens and Pai 2000]. The exact computation of the switching instants is a time consuming task, as additional algorithms, such as the Newton-Raphson method, among others are needed for the exact computation of the switching instants.

In this section, two VSCs models are proposed for the fast and efficient simulation of FACTS devices containing hard-switched Sinusoidal Pulse Width Modulation (SPWM) VSCs.

3.2 Modeling and Simulation of VSCs

The modeling of VSCs using switching functions is not a new issue; in [Lehn 2002], [Lian and Lehn 2006], [Zuñiga-Haro and Ramírez 2009], and [Nabavi-Niaki and Iravani 1996] several models have been reported based on the switching function approach. Under this approach, the power electronic circuit is modeled as a time-varying-topology network. This is a very useful approach at power system level. Usually, power switching devices are modeled as ideal switches; e.g. infinite resistance when the switch is open, and a zero resistance when the switch is closed. Unfortunately, some problems during the solution process can appear, such as numerical oscillations, the need of very small integration steps to achieve a high precision, and inconsistent initial conditions [Vlach, et al. 1995].

The models presented in this chapter are an enhancement of the 6-pulse VSC based on a conventional switching function approach, since we preserve all the advantages of the ideal switch model and eliminate its disadvantages.

Basically, the conventional switching function approach is a special case when the maximum harmonic order in the Fourier model is infinite and when the cutoff frequency is infinite in the hyperbolic tangent model.

The models proposed in this section can be easily incorporated in existing FACTS models, such as those proposed in [Zuñiga-Haro and Ramírez 2009], since multi-pulse arrangements in [Zuñiga-Haro and Ramírez 2009] are achieved by combining several 6-pulse VSCs.

3.3 VSC State Space Representation

The circuit representation of a six-pulse converter is shown in Figure 2.21. According to its mathematical model, this is a discontinuous time-varying system since the switching function S_i instantaneously changes from one state to another. Under these conditions, the conventional numerical integration does not give numerical solutions to a high precision due to the discontinuity.

To alleviate these problems, in this chapter two models for the representation of the VSC are proposed; one is based on a Fourier series expansion and the other is based on a hyperbolic tangent function of the switching function. It will be shown that with the proposed approaches, the numerical integration process can use larger integration steps, as the discontinuities produced by the commutation process no longer exist.

In the next section, the two proposed models for the fast and efficient simulation of VSC power converters are detailed.

3.4 Sinusoidal Pulse-Width Modulation Converter Representation

3.4.1 Fourier Model

It can be observed that the switching function S shown in Figure 2.24(b) contains discontinuities at each switching instant. The discontinuities produced during the commutation process are avoided if a smoother pulse train S_f obtained with the Fourier series replaces S in (2.25) and (2.32a).

The switching instants t_s are obtained with the solution of the nonlinear algebraic equations set describing the sawtooth waveform and v_s . In principle, the computation of the switching instants requires the application of an iterative process for the solution of the nonlinear algebraic equations. However, v_s can be approximated through a first order Taylor series, to allow the original nonlinear algebraic system to be transformed into a linear algebraic system. Let's t_k be the approximated switching instants. The equations defining the straight lines with positive slope for the triangular signal of Figure 2.24(a) are given by,

$$y_{pk} = m_p \left(t - \frac{(k-1)T}{2m_f} \right); \text{ for } \frac{4(k-1)+1}{4m_f}T < t \leq \frac{4(k-1)+3}{4m_f}T \quad (3.1)$$

The equations defining the straight lines with negative slope for the triangular signal are given by,

$$y_{nk} = -m_p \left(t - \frac{(k-1)T}{m_f} \right); \text{ for } \frac{4(k-1)-1}{4m_f}T < t \leq \frac{4(k-1)+1}{4m_f}T \quad (3.2)$$

where T is the fundamental period of v_s , and m_p is the positive slope, calculated as,

$$m_p = \frac{4m_f}{T} \quad (3.3)$$

The control signal v_s is given by,

$$v_s = E_s \cos(\omega t + \theta) \quad (3.4)$$

its first order Taylor approximation around $t=a_k$ is

$$v_s \approx E_s \cos(\omega a_k + \theta) - E_s \sin(\omega a_k + \theta) \omega (t_k - a_k) \quad (3.5)$$

For instance, the switching instant t_1 for $0 < t \leq T/4m_f$ is computed through

$$E_s \cos(\omega a_1 + \theta) - E_s \sin(\omega a_1 + \theta) \omega (t_1 - a_1) = -m_p t_1 \quad (3.6)$$

with $a_1 = 0$, then

$$t_1 = \frac{\cos(\theta)}{\sin(\theta)\omega - \frac{m_p}{E_s}} \quad (3.7)$$

For $T/4m_f < t \leq 3T/4m_f$, with $a_2 = T/2m_f$, we obtain,

$$t_2 = \frac{\cos(a_2\omega + \theta) + \sin(a_2\omega + \theta)a_2\omega + \frac{m_p}{E_s}a_2}{\sin(a_2\omega + \theta)\omega + \frac{m_p}{E_s}} \quad (3.8)$$

In general, for $k = 1, 2, 3, \dots$

$$t_k = \frac{\cos(a_k\omega + \theta) + \sin(a_k\omega + \theta)a_k\omega + (-1)^k \frac{m_p}{E_s}a_k}{\sin(a_k\omega + \theta)\omega + (-1)^k \frac{m_p}{E_s}} \quad (3.9)$$

where,

$$a_k = \frac{T}{2m_f}k \quad (3.10)$$

Equation (3.9) is the general expression for the approximated computation of the switching instants. Once t_k has been calculated, the pulse train is automatically obtained. The proposed model can be resumed by using an approximation of S in terms of the Fourier series, e.g. S_f , being

$$S_f = A_o + \sum_{k=1}^{n_{\max}} (A_k \cos(k\omega_o t) - B_k \sin(k\omega_o t)) \quad (3.11)$$

where n_{\max} is the highest harmonic order, and

$$A_o = 0.5 \quad (3.12)$$

$$A_k = \frac{1}{k\pi} \sum_n^{2m_f} (-1)^{n+1} \sin(n\omega_o t_n) \quad (3.13)$$

$$B_k = -\frac{1}{k\pi} \sum_n^{2m_f} (-1)^{n+1} \cos(n\omega_o t_n) \quad (3.14)$$

For the balanced case, S_f is calculated for one phase, and for the other phases it is obtained with the appropriate phase angle if m_f is multiple of three. In addition, if m_f is odd the switching function has half-wave symmetry, consequently, all even-numbered harmonics vanish. In addition,

$$t_{n+m_f} = t_n + \frac{1}{2T} \quad (3.15)$$

Using half-wave symmetry property, we only need to compute half of the switching times with (3.15).

It is clear that with this Fourier series approximation, the harmonic number for the analysis can be selected. The harmonic number introduced in the analysis increases the computational effort for each integration step; however, this aspect is compensated with the use of larger integration steps, since the discontinuities no longer exist.

In Figure 3.1 a time domain comparison between the discontinuous switching function and the Fourier approach for different harmonic orders is presented. In Figure 3.1(a) a time domain comparison between S and S_f for a maximum harmonic order of 19 (1140 Hz) is shown, in Figure 3.1(b) for a maximum harmonic order of 113 (6780 Hz), and in Figure 3.1(c) for a maximum harmonic order of 300 (18 kHz), respectively.

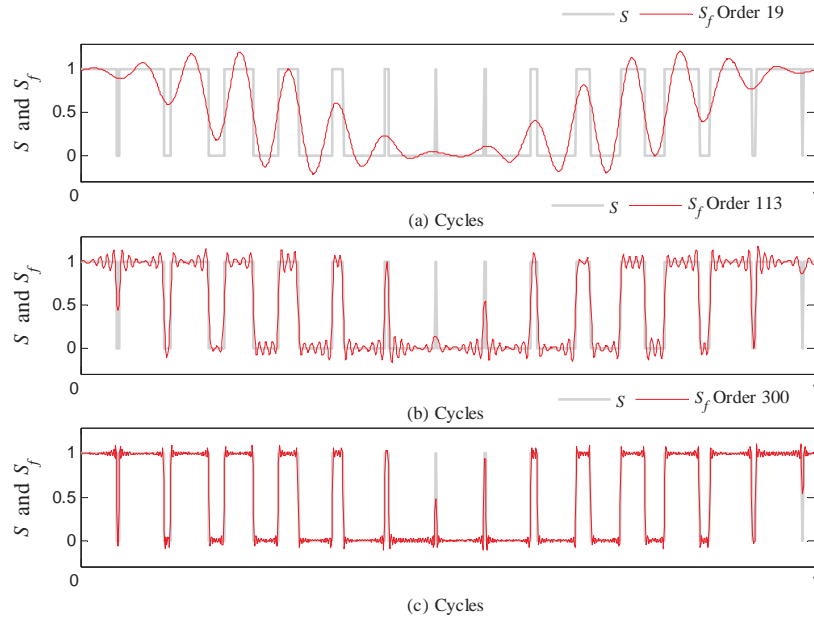


Figure 3.1 Time domain comparison between the discontinuous switching function S and the Fourier approach for different harmonic orders.

Figure 3.2 shows the harmonic domain comparison; in Figure 3.2(a) a harmonic domain comparison between S and S_f for a maximum harmonic order of 19 (1140 Hz) is shown, in

Figure 3.2(b) for a maximum harmonic order of 113 (6780 Hz), and in Figure 3.2(c) for a maximum harmonic order of 300 (18 kHz), respectively. The obtained responses are in close agreement.

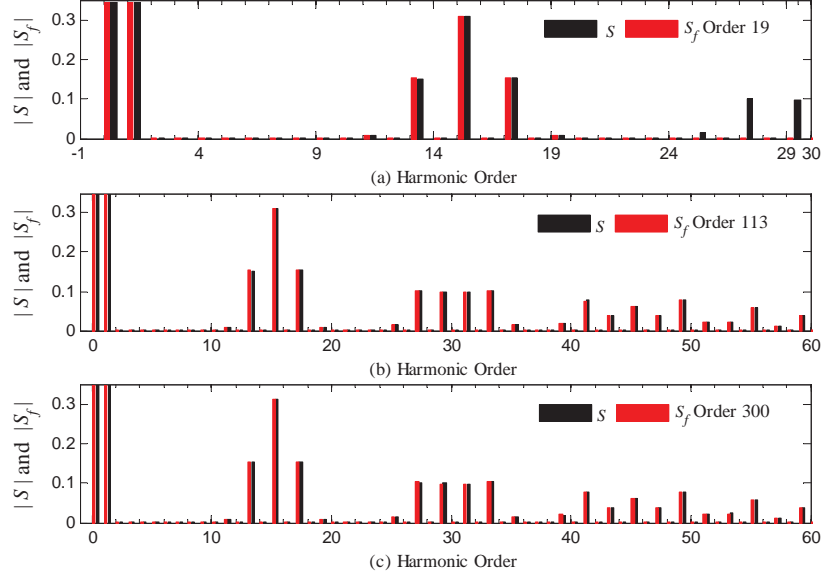


Figure 3.2 Spectrum comparison between the discontinuous switching function S and the Fourier approach for different harmonic orders.

It can be noticed from Figure 3.2 that for a Fourier series approximation with a maximum harmonic order of ζ , the switching function S_f contains up to the harmonic ζ of S , where all the harmonics are included. If higher precision is required, an iterative process can be implemented with (3.9) to increase the precision, so that,

$$t_k^{i+1} = \frac{\cos(t_k^i \omega + \theta) + \sin(t_k^i \omega + \theta) t_k^i \omega + (-1)^k \frac{m_p}{E_s} a_k}{\sin(t_k^i \omega + \theta) \omega + (-1)^k \frac{m_p}{E_s}} \quad (3.16)$$

for $i = 0$, (3.16) corresponds to (3.9). It can be noticed that (3.16) is the iterative Newton method. Expression (3.16) can be also represented as,

$$t_k^{i+1} = t_k^i + \frac{E_s \cos(t_k^i \omega + \theta) - (-1)^k m_p (t_k^i - a_k)}{E_s \sin(t_k^i \omega + \theta) \omega + (-1)^k m_p} \quad (3.17)$$

The harmonic spectrum of (3.11) is finite, for this reason, there are not aliasing problems if the selected integration step is chosen according to the Nyquist criterion. For example, for n_{\max} equal to 51 with a fundamental frequency of 60 Hz, the integration step must be at least 1.634×10^{-4} s. A smaller integration step would be necessary if numerical stability problems are detected, since this integration step is in general large.

3.4.2 Smooth Switching Function

A numerical error is introduced during the numerical integration of electric systems including power electronic switches coming from the discontinuities of the ideal switch model.

If the discontinuities introduced by the switch are avoided, then the numerical error during the integration process can be reduced and high precision in the simulation process can be obtained.

The elimination of the discontinuities in the converter can be achieved by changing the discontinuous commutation signal S by a piecewise commutation signal S_s .

The commutation signal S_s shown in Figure 3.3 satisfies the purpose of avoiding discontinuities. In Figure 3.3(a) S_s versus time is shown, and in Figure 3.3(b) S_s versus u ($u = v_s - tri$).

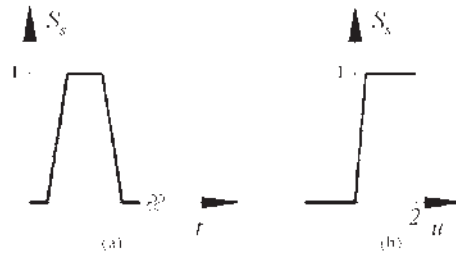


Figure 3.3 Continuous switching function S_s .

3.4.2.1 Selection of m

The selected slope m for S_s determines the maximum harmonic order retained, then, m can be selected to satisfy the maximum harmonic of interest. The spectrum of S is

$$S(\omega) = 2a \frac{\sin(\omega a)}{\omega a} \quad (3.18)$$

It can be observed from (3.18) that the bandwidth of S is infinite. For practical purposes, during the numerical integration process, the switching function S is a discrete function rather than a continuous function. According to the Nyquist-Shannon sampling theorem [Shannon 1998]; if a function $f(t)$ contains no frequencies higher than Ω_c (Hz) this is completely determined by sampling $f(t)$ at a series of samples spaced $1/(2\Omega_c)$ s. Consequently, the highest frequency retained from $f(t)$ by its samples is $f_c/2$, where f_c ($1/\delta t$) is the sampling frequency.

Based on Figure 3.4, where S_n is the discrete representation of S , and since it can be observed that m is defined as

$$m = \frac{1}{\delta t} \quad (3.19)$$

then m is related to the maximum frequency retained during the simulation process by

$$m = 2\Omega_c \quad (3.20)$$

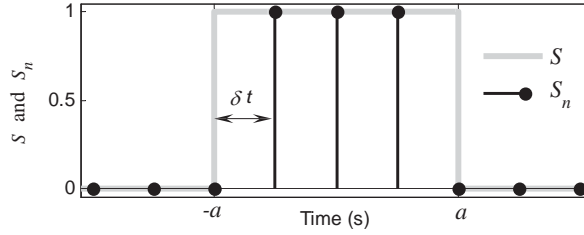


Figure 3.4 Continuous switching function and discrete switching function.

3.4.2.2 Hyperbolic Tangent Model

The proposed switching function S_s shown in Figure 3.3 is continuous; however, it is not differentiable in the corners. To solve this problem, this function can be represented by a smoother function. A continuous and differentiable function that satisfies these conditions is the hyperbolic tangent function,

$$S_{si} = \frac{\tanh(\alpha(v_{si} - tri)) + 1}{2} \quad (3.21)$$

v_{si} is the control signal, $i = a, b, c$, tri is the sawtooth waveform and, α is maximum slope of S_{si} .

The relationship between m and (3.21) is given by

$$m = \max\left(\frac{dS}{dt}\right) = \frac{1}{2}\alpha\left(m_a\omega + \frac{4m_f}{T}\right) \quad (3.22)$$

From (3.20) and (3.22), α can be selected as

$$\alpha = \frac{4\Omega_c}{m_a\omega + \frac{4m_f}{T}} \quad (3.23)$$

m_a is time varying and can take values from 0 to 1 in linear modulation, and larger than 1 when operating in overmodulation. α must be fixed to the maximum value in (3.23), i.e. $m_a=0$,

$$\alpha = \max\left(\frac{4\Omega_c}{m_a\omega + \frac{4m_f}{T}}\right) = \frac{T\Omega_c}{m_f} \quad (3.24)$$

Figure 3.5 shows the approximated commutation functions based on the Fourier series for different harmonic orders, and for different cutoff frequencies Ω_c in the hyperbolic tangent model; e.g. $\Omega_c=1140$ Hz in Figure 3.5(a) and $\Omega_c=6780$ Hz in Figure 3.5(b). Please

notice that both Fourier and hyperbolic tangent approximation, respectively, are in good agreement for the same harmonic order. It is to be remarked how the raising slope in the proposed commutation functions proportionally increases with the inclusion of a higher harmonic order in the approximation. Please observe that the Fourier approximation satisfies this remark, which, besides, agrees with the sampling theorem.

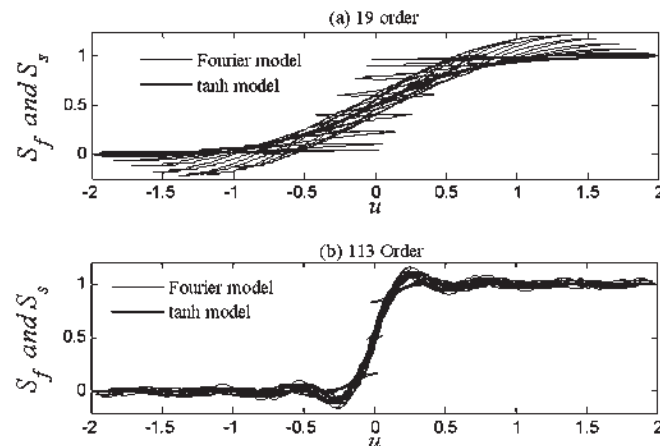


Figure 3.5 Commutation functions S_f and S_s for different harmonic orders and cutoff frequencies.

The spectrum of (3.21) is not finite, and it has aliasing problems, therefore, the Nyquist criterion is not enough to avoid overlapping. Besides, the aliasing problem is not the only error introduced by the approximation of the commutation function with the hyperbolic tangent model, since there is another error due to the rounding corners in the commutation function S_s , for this reason, the frequencies close to Ω_c are not well retained.

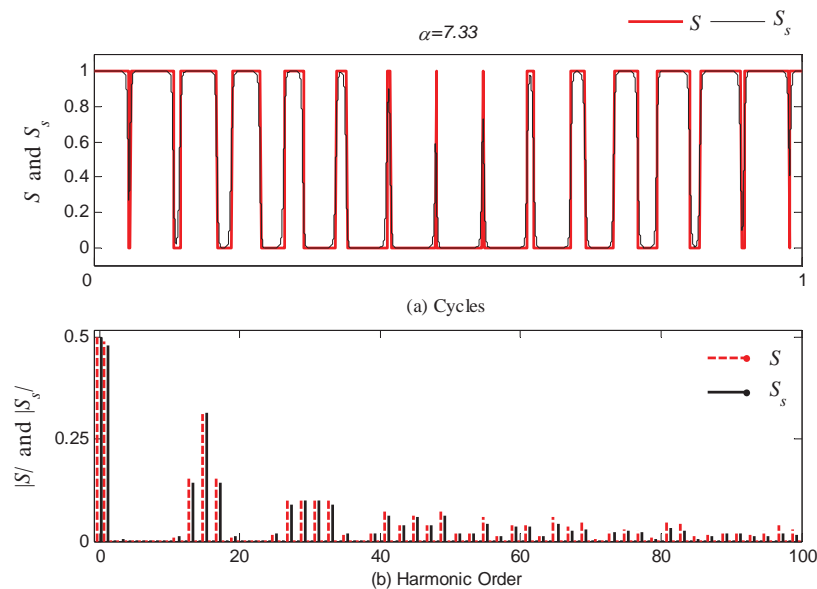


Figure 3.6 Comparison between the discontinuous switching function S and the hyperbolic tangent approach for $\alpha=7.33$. (a) Time domain waveforms, (b) Harmonic spectrum.

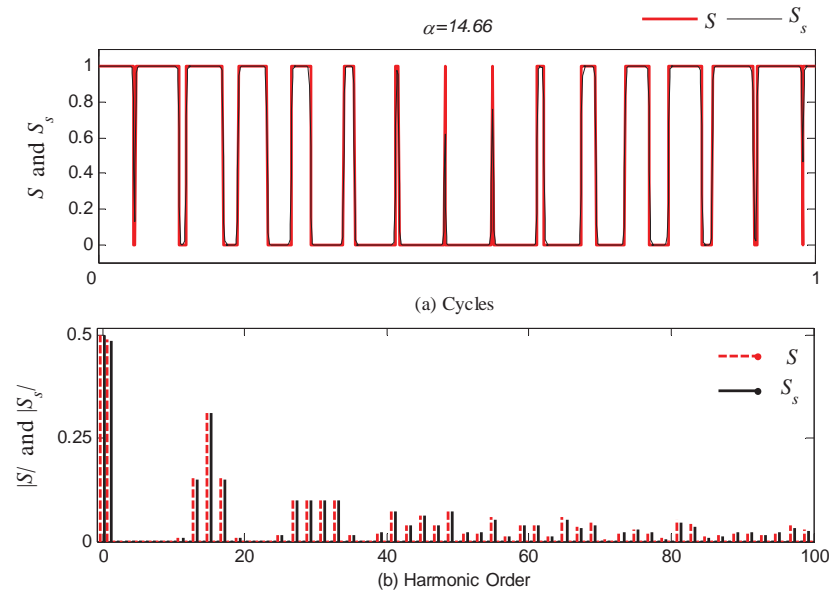


Figure 3.7 Comparison between the discontinuous switching function S and the hyperbolic tangent approach for $\alpha=14.66$. (a) Time domain waveforms, (b) Harmonic spectrum.

To alleviate this problem, α can be fixed at a higher value than that obtained in (3.24). A comparison between the commutation functions S and S_s for $\Omega_c=6.6$ kHz, which is equivalent to the first 110 harmonics with a fundamental frequency of 60 Hz is shown in Figure 3.6 for $\alpha=7.33$, and in Figure 3.7 for $\alpha=14.66$, respectively. Please notice from Figure 3.6(a) that the waveform in time S is closely followed by S_s ; however, the spectrum in Figure 3.6(b) is only well retained up to the harmonic 40th. This error is due to the rounding corners in the commutation function S_s . For this case, α is computed directly from (3.24), e.g. $\alpha=7.33$. In Figure 3.7(a) the waveforms in the time domain are very close to each other. Besides, the first 110 harmonics contained in S are contained in S_s . For this case, α is computed as twice the value obtained with (3.24), e.g. $\alpha=14.66$.

3.5 Solution Comparisons and Results Validation

In this section, the proposed commutation functions are applied to analyze the performance of three FACTS devices based on VSCs. The results obtained with the proposed models of the VSC are validated against those obtained with Simulink [TEQSIM International Inc 2001], and PSCAD/EMTDC [HVDC Research Centre 2003].

Power System Blockset (PSB) for use with Matlab/Simulink employs state-variable analysis, whereas, PSCAD/EMTDC is based on analysis nodal using Northon equivalents based on difference equations. The difference equations set is obtained by discretization of the original ODE set using the trapezoidal rule. In PSB more complex control algorithms can be implemented into the models in an easier and faster way than using PSCAD/EMTDC. Besides, PSB can use several Matlab toolboxes. In particular, it has the PWM generator and the VSC blocks. In general terms, both programs are suitable for transient analysis of power electronic components and are very easy to use. The main advantage of the PSB is that it is developed in Matlab/Simulink environment, this fact

makes possible to use it together with several other control design tools. On the other hand, the main advantage of the PSCAD/EMTDC is the computing time. In this software the simulations run very fast. However, it is possible to use the Simulink Accelerator and the Real-Time Workshop to improve the PSB performance; a C code is generated. Additionally, the PSB can use several integration methods, meanwhile PSCAD/EMTDC only uses the trapezoidal rule.

The test case is shown in Figure 3.8. In this circuit there are two VSCs; one is connected in series, and the other is shunt connected. There is a dc link capacitor between both VSCs. Both VSCs operating together constitute the UPFC. The series VSC constitutes the SSSC, and the shunt VSC the STATCOM. The series and shunt transformer are represented by RL branches, whose impedance is $0.018+j0.34$ pu. In the test system circuit breakers have been included to allow the reconfiguration of the system. The base power is 5 kVA and the base voltage is 166.6 Volts. For more details of this study case see Appendix A.

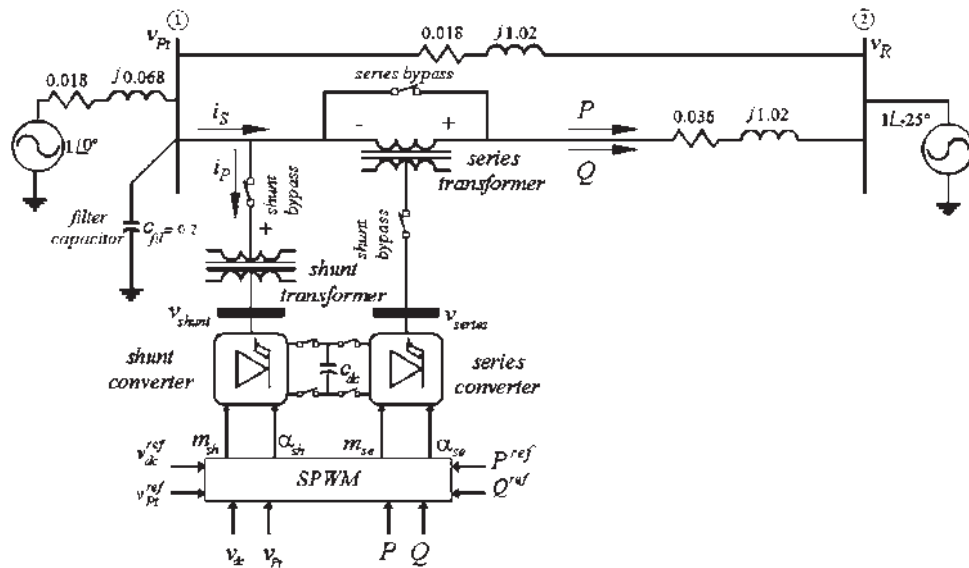


Figure 3.8 Single-phase test system.

The periodic steady-state solution is achieved once the difference between two successive state vectors at the beginning and at the end of one period is within a specific tolerance, e.g. 10^{-10} pu.

3.5.1 Static Compensator (STATCOM)

The STATCOM includes the control system described in [Mahyavanshi and Radman 2006]. The initial conditions are zero, the reference line to line voltage is 0.975 pu at node 1, and the reference voltage for the dc capacitor is 2 pu. The modulation index is $m_f = 15$. The maximum harmonic order in the Fourier approach is 51 (3060 Hz).

In Figure 3.9(a) the convergence error in reference to the steady state solution obtained with PSCAD/EMTDC using different integration steps is shown. The convergence error at the cycle $n+1$ is computed as $\max(\text{abs}(\mathbf{x}(nT) - \mathbf{x}(nT+T)))$, where T is the period of the limit cycle. An error of the order of 10^{-5} is achieved when δt is at least $0.1 \mu\text{s}$ and the

interpolation option is enabled; a similar behavior is observed with Simulink. A still smaller integration step would be needed to ensure a reliable harmonic evaluation. On the other hand, the convergence errors to the steady state solution obtained with the proposed models are shown in Figure 3.9(b). Notice that the proposed models achieve high precision even for large integration steps, e.g. 110 μs for the Fourier model, and 33 μs for the hyperbolic tangent model.

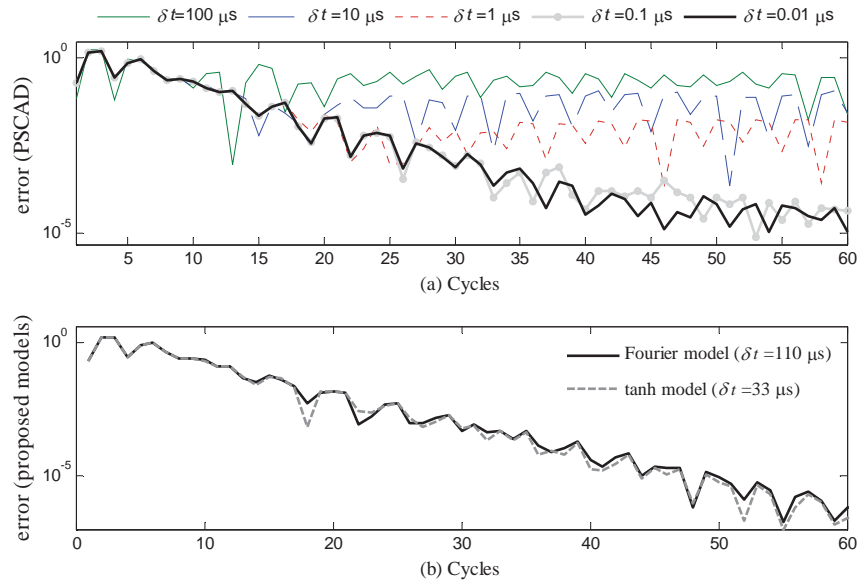


Figure 3.9 Convergence error for the STATCOM. (a) PSCAD/EMTDC solution using the ideal switch model. (b) Solution obtained using the proposed models.

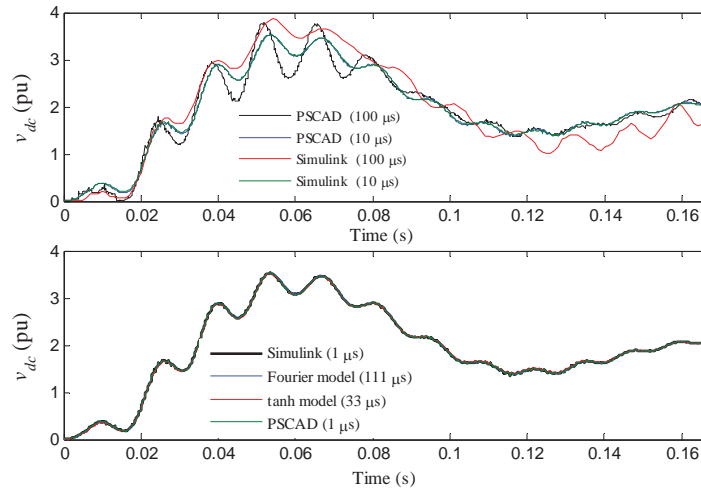


Figure 3.10 Transient solution comparison for the STATCOM (a) Transient solution computed using Simulink and PSCAD/EMTDC for the STATCOM. (b) Transient solution comparison for the STATCOM between Simulink, PSCAD/EMTDC, and the proposed models.

Figure 3.10(a) shows the transient solutions for the dc capacitor voltage computed with Simulink and PSCAD/EMTDC. Notice that this solution is very sensitive to the integration step and it is necessary to use a very small integration step to obtain a reliable solution.

Figure 3.10(b) shows a comparison between the transient solution obtained with Simulink, the Fourier approach, the hyperbolic tangent model, and PSCAD/EMTDC. It can be observed that these solutions are in very close agreement.

The integration step needed by Simulink is $1 \mu\text{s}$, the Fourier model needs $111 \mu\text{s}$, the hyperbolic model $33 \mu\text{s}$, and PSCAD/EMTDC $1 \mu\text{s}$. The integration step needed by the Fourier approach is 111 times larger than that used by Simulink and PSCAD/EMTDC, meanwhile, the integration step of the hyperbolic tangent model is 33 times larger than the integration step used by Simulink and PSCAD/EMTDC.

A comparison between the periodic steady state solution obtained with Simulink, the Fourier model, the hyperbolic tangent model, and PSCAD/EMTDC is presented in Figure 3.11. Figure 3.11(a) shows the voltage at the dc capacitor v_{dc} , Figure 3.11(b) the voltage v_{P1a} at phase A of node 1, and Figure 3.11(c) the series current of phase A i_{Sa} . An integration step of $0.1 \mu\text{s}$ has been used in Simulink and PSCAD/EMTDC, $100 \mu\text{s}$ with the Fourier model, and $30 \mu\text{s}$ with the hyperbolic tangent model, respectively. Notice that all solutions are in very good agreement.

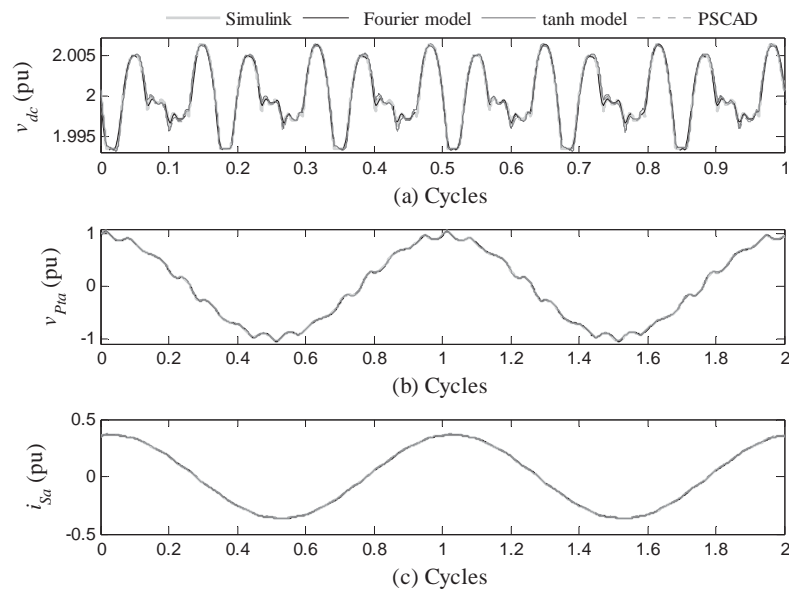


Figure 3.11 Steady state solution comparison for the STATCOM.

Further correlation between the solution obtained with Simulink, PSCAD/EMTDC and the proposed models is illustrated in Figure 3.12, e.g. the harmonic spectrum for the dc voltage capacitor v_{dc} in Figure 3.12(a), the voltage of phase A at the node 1 v_{P1a} in Figure 3.12(b), and the series current of phase A i_{Sa} in Figure 3.12(c), respectively. Observe that the obtained harmonic spectrum is in very good agreement.

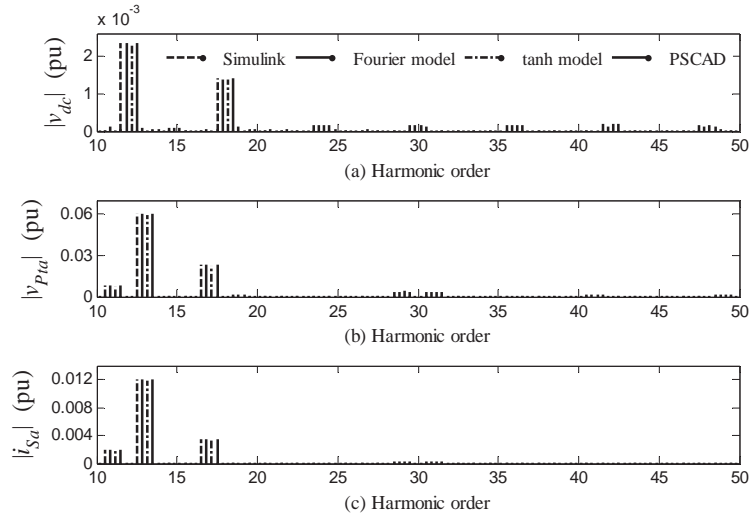


Figure 3.12 Harmonic content comparisons. (a) Harmonic content in the dc voltage. (b) Magnitude of selected harmonics in phase A of the terminal voltage. (c) Magnitude of selected harmonics in phase A of the series current.

3.5.2 Static Synchronous Series Compensator (SSSC)

The SSSC includes the control system shown in Figure 3.13. This control has to control objectives: to control the active power (P) that flows in the transmission line connected in series with the SSSC, and to maintain the dc voltage capacitor at its reference value. Remember that the SSSC does not interchange active power in steady-state, only the power loss; otherwise the dc capacitor is discharged. In transient state the SSSC has transient interchanges of active power with the network, which is reflected in variation of the dc voltage. Under this situation, the control regulates the interchange of active power in order to maintain the dc voltage capacitor at its steady-state. The initial conditions are zero; the active power reference P^{ref} is 1 pu, and the index modulation is 21. P^{ref} is the active power reference in the transmission line in series with the SSSC. The maximum harmonic order of the Fourier series model is 69 (4140Hz).

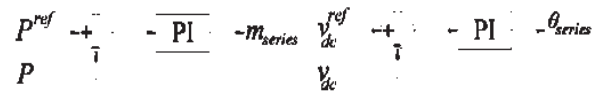


Figure 3.13 SSSC control.

Figure 3.14 shows the transient solution comparison for the dc voltage capacitor. This solution has been computed using Simulink, and the two proposed models. An integration step of $0.1\mu s$ has been used in Simulink, $100\mu s$ for the Fourier approach method, $30\mu s$ for the hyperbolic tangent model, and $0.1\mu s$ in PSCAD/EMTDC. Observe that the proposed models closely agree with the solution obtained with Simulink and PSCAD/EMTDC.

A comparison between the periodic steady-state solutions is shown in Figure 3.15; the capacitor voltage v_{dc} is shown in Figure 3.15(a), the terminal voltage at node 1 v_{Pta} in Figure 3.15(b), and the phase A of the series current i_{Sa} in Figure 3.15(c), respectively. Observe that all solutions are again in very close agreement.

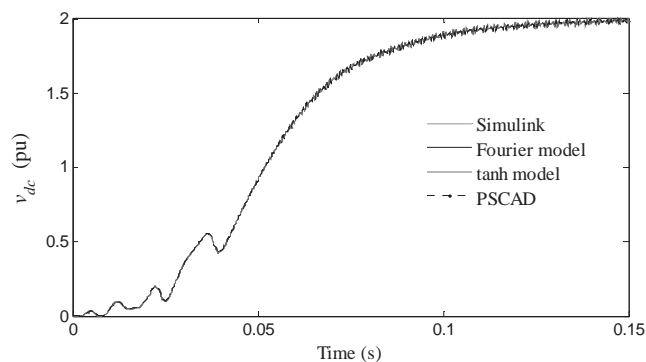


Figure 3.14 Transient solution comparison for the SSSC.

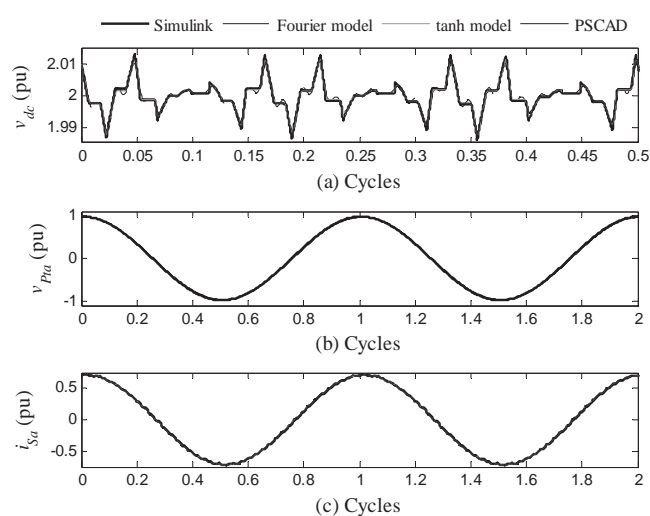


Figure 3.15 Steady state solution comparison for the SSSC.

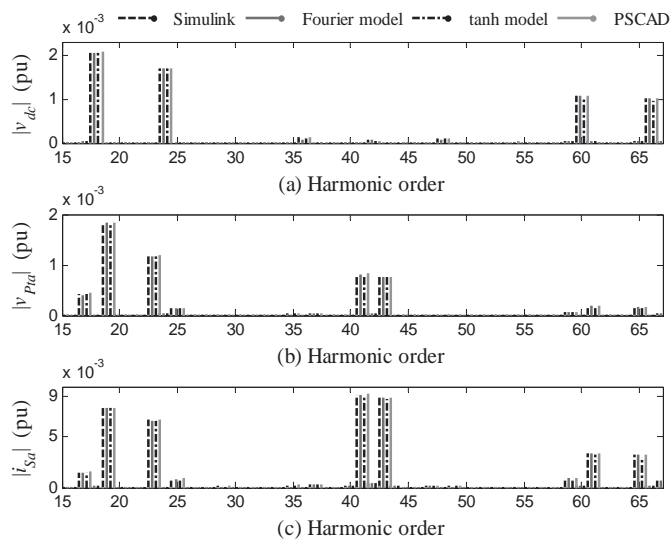


Figure 3.16 Harmonic content comparisons. (a) Harmonic content in the dc voltage. (b) Magnitude of selected harmonics in phase A of the terminal voltage. (c) Magnitude of selected harmonics in the phase A of the series current.

Figure 3.16(a) shows the harmonic content for v_{dc} , in Figure 3.16(b) for v_{P1a} , and in Figure 3.16(c) for i_{Sa} . It can be seen that the proposed models are in very good agreement with the solution obtained with Simulink and PSCAD/EMTDC.

3.5.3 Unified Power Flow Controller (UPFC)

The UPFC includes the shunt control described in [Mahyavanshi and Radman 2006], and the series control proposed in [Fujita, et al. 2001]. The initial condition is zero, except for the dc capacitor voltage, which is 2 pu. The series controller regulates the real ($P_{ref}=0.9$ pu) and reactive ($Q_{ref}=0$ pu) power flows by adjusting the injected series voltage. The shunt converter regulates the dc-side capacitor voltage ($v_{dc}=2$ pu) and the sending end voltage ($v_{P1}=0.96$ pu). The modulation index is $m_f=9$. The maximum harmonic order in the Fourier approach is 69 (4140 Hz).

Figure 3.17 shows the transient solution comparison for the capacitor voltage of the UPFC operating in open-loop control. For this operating mode, the initial condition has been assumed zero. This solution has been computed using Simulink, PSCAD/EMTDC and the two proposed models. An integration step of $0.1\mu\text{s}$ has been used in Simulink and PSCAD/EMTDC, $80\mu\text{s}$ for the Fourier approach method, and $30\mu\text{s}$ for the hyperbolic tangent model.

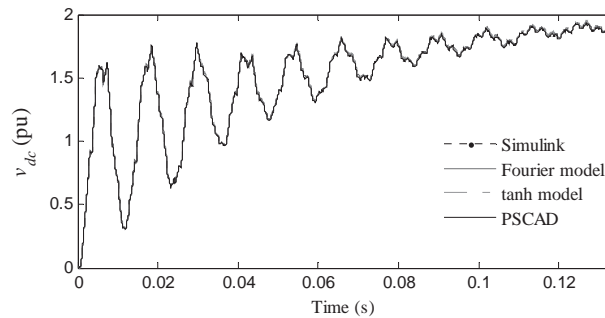


Figure 3.17 Transient solution comparison for the UPFC.

A comparison between the periodic steady state solution obtained with Simulink, the Fourier model, the hyperbolic tangent model, and PSCAD/EMTDC is shown in Figure 3.18. Figure 3.18(a) shows the capacitor voltage v_{dc} , Figure 3.18(b) shows the voltage of phase A v_{P1a} in bus 1, and Figure 3.18(c) shows the series current of phase A i_{Sa} . The slight difference between the solution obtained with PSCAD/EMTDC and the other solutions is because the UPFC implemented in PSCAD/EMTDC is operating in open-loop control, meanwhile, the other solutions are operating in closed-loop control; however, all the solutions are in good agreement.

A validation of the proposed models is further illustrated in Figure 3.19, which shows the harmonic spectrum for the capacitor voltage v_{dc} in Figure 3.19(a), the voltage of phase A at node 1 in Figure 3.19(b), and the phase A of the series current in Figure 3.19(c), respectively; all the solutions are in excellent agreement.

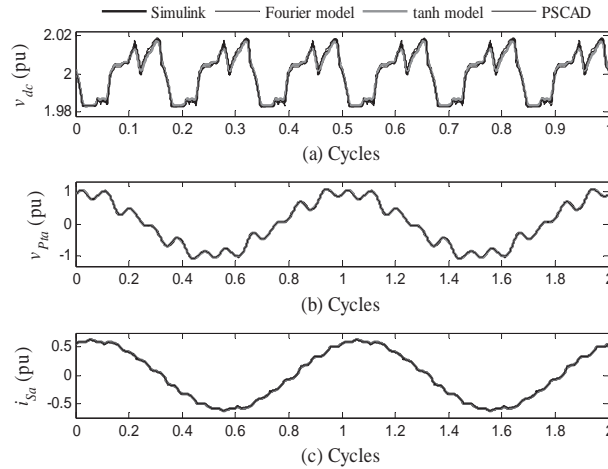


Figure 3.18 Steady-state solution comparison for the UPFC.

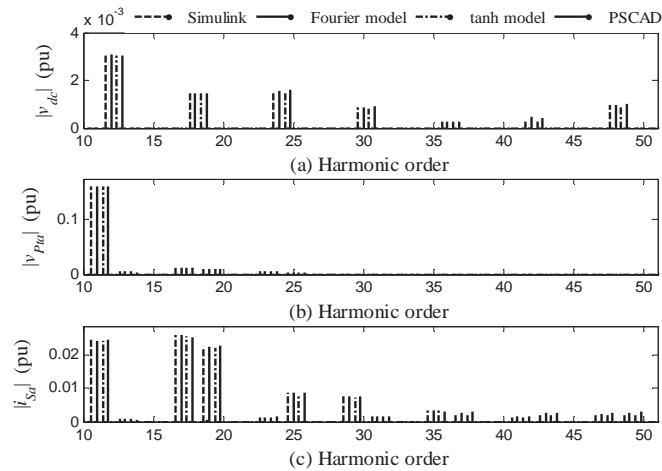


Figure 3.19 Harmonic content comparisons. (a) Harmonic content in the dc voltage. (b) Magnitude of selected harmonics in phase A of the terminal voltage. (c) Magnitude of selected harmonics in the phase A of the series current.

3.6 Distribution Static Compensator

3.6.1 Distribution Network including the DSTATCOM

In order to cancel-out unbalance or harmonics in the line current the voltage source converter that constitutes the DSTATCOM must be able to inject currents in one phase independently of the other two phases. From this point of view the structure of a DSTATCOM is very important. The DSTATCOM structure adopted in our analysis is shown in Figure 3.20.

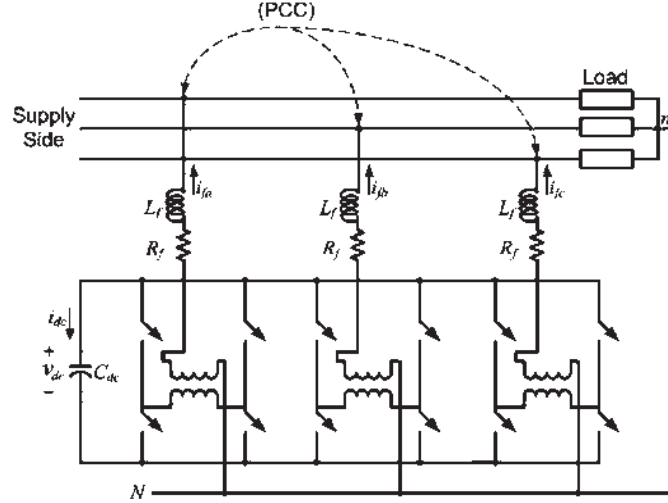


Figure 3.20 Structure of the DSTATCOM.

The structure shown in Figure 3.20 contains three H-bridge voltage source converters connected to a common dc storage capacitor. Each VSC is connected to the network through a transformer. The purpose of including the transformers is to provide isolation between the inverter legs. This prevents the dc capacitor from being shorted through switches of the different inverters. The structure shown in Figure 3.20 allows three independent current injections. It is to be noted that due to the presence of transformers, this topology is not suitable for canceling any dc component in the load current [Ghosh and Ledwich 2003]. The inductance L_f represents the leakage inductance of each transformer and additional external inductance, if any. The switching losses of an inverter and the copper loss of the connecting transformer are represented by a resistance R_f . For more details about this structure please see [Ghosh and Ledwich 2003]. This converter topology is used in this thesis for the DSTATCOM operating in voltage and current mode; however, the converter topology shown in Figure 2.15, among other, can be used.

Now, let us consider the following nonlinear system periodically excited with a T -periodic function, which can describe the dynamic behavior of the equivalent circuit of the compensated system shown in Figure 3.21.

$$\dot{\mathbf{x}}(t) = \mathbf{f}(t, \mathbf{x}; \mathbf{M}) \quad (3.25)$$

where \mathbf{x} and \mathbf{f} are n -dimensional vectors and \mathbf{M} is a m -dimensional parameter vector.

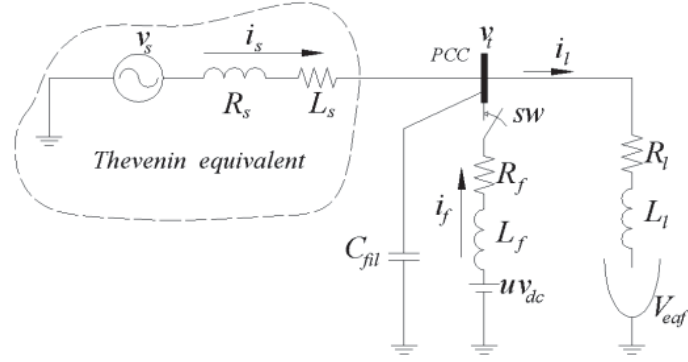


Figure 3.21 Compensation of the EAF when the source is non-stiff and the DSTATCOM contains a passive filter.

In particular, for the electric system shown in the Figure 3.21, the function \mathbf{f} is defined as

$$\mathbf{f}(t, \mathbf{x}; \mathbf{M}) = \begin{pmatrix} -\frac{R_s}{L_s} i_s - \frac{1}{L_s} v_t + \frac{v_s}{L_s} \\ \frac{1}{C_{fil}} i_s - \frac{1}{C_{fil}} i_t + \frac{1}{C_{fil}} i_f \\ -\frac{R_l}{L_l} i_t + \frac{1}{L_l} v_t - \frac{V_{eaf}}{L_l} \\ -\frac{R_f}{L_f} i_f - \frac{1}{L_f} v_t + \frac{V_{dc} u}{L_f} \end{pmatrix} \quad (3.26)$$

the state vector is defined as

$$\mathbf{x}' = [i_s \quad v_t \quad i_t \quad i_f] \quad (3.27)$$

where $'$ is the transpose operator.

The nonlinear load is an electric arc furnace; however, a different load can be connected to the PCC. The dynamic behavior of the $v - i$ characteristic of the EAF is described by the differential equation introduced in [Acha, et al. 1990]. This differential equation is based on the principle of energy balance. Starting from the power balance equation for the electric arc, the following differential equation is derived in [Acha, et al. 1990]:

$$K_1 r^n + K_2 r \frac{dr}{dt} = \frac{K_3}{r^{m+2}} i_t^2 \quad (3.28)$$

Here the arc radius r is chosen as state variable. The arc voltage V_{eaf} is given by

$$V_{eaf} = \frac{i_t}{g} \quad (3.29)$$

where g is the arc conductance and given by the following equation:

$$g = \frac{r^{m+2}}{K_3} \quad (3.30)$$

It is possible to represent the different stages of the arcing process by simply modifying the parameters of m and n in (3.28). The complete set of combinations of these parameters for different stages of the electric arc can be found in [Acha, et al. 1990].

In the detailed model the switches are IGBTs/diodes, the hysteresis modulation scheme, and the dc circuit are explicitly represented. The implementation of the three H-bridge converters and their switching control can be directly done in any EMTP-type simulator. In this thesis, the DSTATCOM detailed model has been implemented in Power BlockSet/SIMULINK [TEQSIM International Inc 2001].

In bifurcation analysis, the detailed model is not suitable because of the difficulty to compute to a high precision the limit cycle, and for assessing its stability. For this reason, we propose a simplified model for the DSTATCOM operating in voltage and current mode, respectively, in which all the difficulties above mentioned are avoided. In the proposed representation, the three H-bridges for the DSTATCOM operating in current control mode are represented through controlled current sources, meanwhile the three H-bridges for the DSTATCOM operating in voltage control mode are represented through controlled voltages sources, the link between the dc side and the ac side is well represented using the energy preservation principle.

3.6.2 DSTATCOM Operating in Current Control Mode

The DSTATCOM is a shunt connected device similar to the static compensator (STATCOM) [Hingorani and Gyudyi 2000]. However, there are important differences in the operating characteristic between the DSTATCOM and the STATCOM. The STATCOM injects a set of three balanced quasi-sinusoidal voltages. On the other hand, the DSTATCOM must be able to inject an unbalanced and harmonically distorted current. Therefore, its control is significantly different from that of a STATCOM.

In the current control mode, the DSTATCOM compensates for any unbalance or distortion in the load, thus, the load draws a balanced current from the system irrespective of any unbalance or harmonic distortion in the load [Ghosh and Ledwich 2003]. One of the most important issues for the load compensation is the generation of the reference compensator currents. There are several techniques proposed; [Ghosh and Ledwich 2003], [Ghosh and Joshi 1998], [Akagi, et al. 1984], [Akagi, et al. 1986], [Ghosh and Joshi 2000], and [Mishra, et al. 2003]. However, most of these methods assume that the voltage at the PCC is stiff. Unfortunately this is not a valid assumption for most practical applications.

For this thesis, the computation of the reference currents will be done using instantaneous symmetrical components [Ghosh and Joshi 1998]. In addition, the source is not assumed to be stiff.

3.6.2.1 Compensation Algorithm and Control

In (3.26), u is the control signal constrained between +1 and -1. Once the reference currents are generated, they are tracked-down in a hysteresis band current control scheme. The control signal is computed through,

$$u = \text{hys}(i_f - i_f^*) \quad (3.31)$$

where i_f^* is the reference compensation current. These are given by [Ghosh and Joshi 1998],

$$\left. \begin{aligned} i_{fa}^* &= i_{la} - \frac{v_{ia} + (v_{ib} - v_{ic})\beta}{\sum_{x=a,b,c} v_{tfx}^2} (P_l^{av} + P_{loss}) \\ i_{fb}^* &= i_{lb} - \frac{v_{ib} + (v_{ic} - v_{ia})\beta}{\sum_{x=a,b,c} v_{tfx}^2} (P_l^{av} + P_{loss}) \\ i_{fc}^* &= i_{lc} - \frac{v_{ic} + (v_{ia} - v_{ib})\beta}{\sum_{x=a,b,c} v_{tfx}^2} (P_l^{av} + P_{loss}) \end{aligned} \right\} \quad (3.32)$$

where β is computed based on the load power factor.

In (3.32), P_l^{av} is the average power drawn by the load, P_{loss} is the power loss due to R_f , and v_{tfx} is the fundamental component of v_{tx} , for $x = a, b, c$.

The hysteresis function hys is defined by,

$$\text{hys}(w) = \begin{cases} 1 & \text{for } w \leq -h \\ -1 & \text{for } w > h \end{cases} \quad (3.33)$$

where $2h$ is the hysteresis band.

The power loss P_{loss} is computed through the proportional controller [Ghosh and Ledwich 2003], e.g.

$$P_{loss} = K_{pdc} (v_{dc}^* - v_{dc}^{av}) + K_{idc} \int (v_{dc}^* - v_{dc}^{av}) dt \quad (3.34)$$

where v_{dc}^* is the reference dc voltage, v_{dc}^{av} is the average voltage across the dc capacitor.

To compute β , we introduce a simple *proportional-integral* control given by,

$$\beta = K_{p\beta} (\beta_t^* - \beta_t) + K_{i\beta} \int (\beta_t^* - \beta_t) dt \quad (3.35)$$

where

$$\beta_i^* = \tan\left(\cos^{-1}(PF^*)\right) / \sqrt{3} \quad (3.36)$$

$$\beta_i = \tan\left(\cos^{-1}(PF)\right) / \sqrt{3} \quad (3.37)$$

and PF^* is the desired reference power factor at the PCC bus and PF is the load power factor at PCC.

3.6.2.2 Simplified DSTATCOM Model

In the detailed model, the switching elements are explicitly represented. The modeling of the switching devices can be performed with different levels of detail. A very detailed model can be justified and necessary when the phenomena associated with the switching process are to be analyzed, albeit at a high computational cost. On the other hand, for power systems studies, usually the study of the switching phenomena, this is not necessary. Thus, it is advantageous to model the switches as open and short circuits. However, this model has some disadvantages; for example, inconsistent initial conditions can appear [Vlach, et al. 1995]. One way to mitigate the adverse effects related to the switching process is to use a small integration time step to carry-out the simulation. However, it takes a long simulation time.

The source of numerical problems for the integration process arises from the discontinuities and the non-differentiability introduced by the ideal switch model [Banerjee and Verghese 2001] [Mohan, et al. 1995].

In Figure 3.22 the schematic representation of the simplified DSTATCOM model in current control mode is shown. Figure 3.23 shows the schematic representation of the dc link model. The power balance between the dc and ac side can be given as,

$$P_{dc} = v_{dc} i_{dc} = i_{fa} v_{ta} + i_{fb} v_{tb} + i_{fc} v_{tc} + R_f (i_{fa}^2 + i_{fb}^2 + i_{fc}^2) + L_f \left(i_{fa} \frac{di_{fa}}{dt} + i_{fb} \frac{di_{fb}}{dt} + i_{fc} \frac{di_{fc}}{dt} \right) \quad (3.38)$$

where

$$\frac{di_{fa}}{dt} = -\frac{\Delta \left(\frac{dv_{ta}}{dt} + \left(\frac{dv_{tb}}{dt} - \frac{dv_{tc}}{dt} \right) \beta + (v_{tb} - v_{tc}) \frac{d\beta}{dt} \right) + \frac{d\Delta}{dt} (P_l^{av} + P_{loss})}{\Delta^2} + \frac{di_{ta}}{dt} - \frac{v_{ta} + (v_{tb} - v_{tc}) \beta}{\Delta} \left(\frac{dP_{dc}}{dt} + \frac{dP_{loss}}{dt} \right) \quad (3.39)$$

$$\frac{di_{fb}}{dt} = -\frac{\Delta \left(\frac{dv_{tb}}{dt} + \left(\frac{dv_{tc}}{dt} - \frac{dv_{ta}}{dt} \right) \beta + (v_{tc} - v_{ta}) \frac{d\beta}{dt} \right) + \frac{d\Delta}{dt} (P_l^{av} + P_{loss})}{\Delta^2} + \frac{di_{tb}}{dt} - \frac{v_{tb} + (v_{tc} - v_{ta}) \beta}{\Delta} \left(\frac{dP_{dc}}{dt} + \frac{dP_{loss}}{dt} \right) \quad (3.40)$$

$$\frac{di_{fc}}{dt} = -\frac{\Delta \left(\frac{dv_{tc}}{dt} + \left(\frac{dv_{ta}}{dt} - \frac{dv_{tb}}{dt} \right) \beta + (v_{ta} - v_{tb}) \frac{d\beta}{dt} \right) + \frac{d\Delta}{dt} (P_l^{av} + P_{loss})}{\Delta^2} + \frac{di_{tc}}{dt} - \frac{v_{tc} + (v_{ta} - v_{tb}) \beta}{\Delta} \left(\frac{dP_{dc}}{dt} + \frac{dP_{loss}}{dt} \right) \quad (3.41)$$

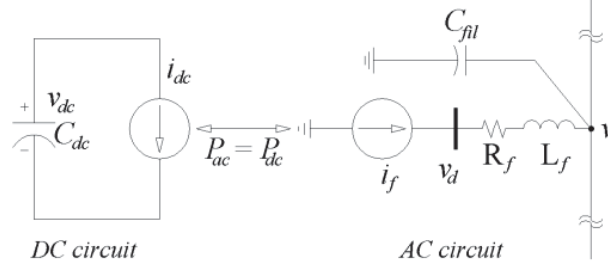


Figure 3.22 Schematic representation for the simplified model.

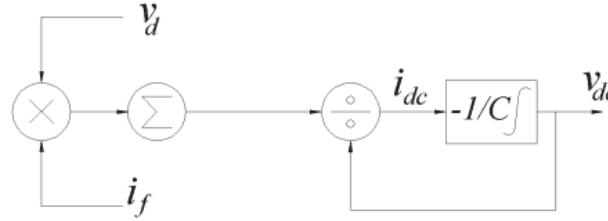


Figure 3.23 dc link model.

From (3.38), the dc current i_{dc} is computed as the ac power divided by the dc voltage capacitor v_{dc} . Thus, this simplified model based on the energy preservation principle is limited for $v_{dc} \geq 0$.

3.6.2.3 Comparative Analysis of Models for the DSTATCOM in Current Mode

In this section, the performance of the simplified model presented in Section 3.6.2.2 is compared against the detailed model where the voltage source inverter based on the three H-bridge inverter is used. The test system is shown in Figure 3.21. The system parameters and the DSTATCOM parameters are given in Table 3.1. The hysteresis band for the detailed model is $h=1$ A.

TABLE 3.1 SYSTEM PARAMETERS OF THE DSTATCOM IN CURRENT MODE

Systems Parameters	DSTATCOM
System voltage ($ V_s $): 440 Volts (peak).	Voltage controllers gains of dc capacitor loops: $K_{pdc}=80$, $K_{idc}=500$.
Feeder impedance (R_s, L_s): $1+j 7.54 \Omega$	β control loop gains: $K_{p\beta}=0.5$, $K_{i\beta}=300$.
ac capacitor (C_{dc}): 70 μF	dc capacitor(C_{dc}): 1500 μF
Feeder load impedance (R_l, L_l): $0.5+j 3.77 \Omega$	Interface circuits (R_f, L_f): $0.05+ j 3.77 \Omega$
EAF constants: $K_1=15$, $K_2=0.05$, $K_3=800$, $m=0$ and $n=2$.	Reference value of dc capacitor voltage: 1200 Volts

Initially, for $t < 0$ the switch sw is open and the electric circuit is in periodic steady-state. At $t = 0$ s the switch sw is closed and the DSTATCOM starts the compensation with the dc capacitor pre-charged at 1200 Volts. Selected waveforms are presented in Figure 3.24 and Figure 3.25. Figure 3.24 shows the steady-state solution of the power loss P_{loss} , with different integration steps in the detailed model and with an integration step of 65 μs for the simplified model. From this Figure it is easy to notice that if the commutation process has

to be taken into account, a very small integration step size ($0.52 \mu\text{s}$) should be chosen with the detailed model, otherwise, the solution will contain a large numerical error due to the commutation process. Figure 3.25(a) shows the compensation current i_{fa} , while Figure 3.25(b) shows the dc voltage v_{dc} with the simplified model and with the detailed model for an integration step size of $65 \mu\text{s}$ and $1 \mu\text{s}$, respectively. A good agreement between the two models has been achieved, even though the simplified model has a considerably larger integration step size (125 times).

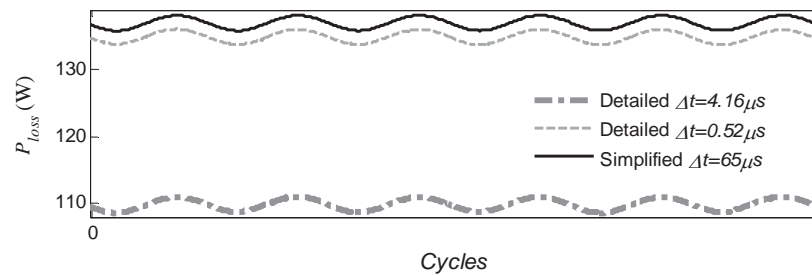


Figure 3.24 Comparison in the time domain between the detailed and the simplified model for P_{loss} in steady-state for different integration steps.

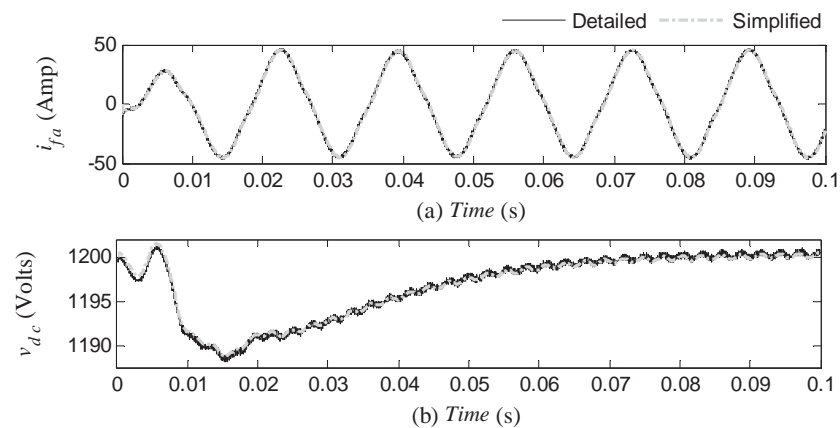


Figure 3.25 Comparison in the time domain between the detailed and the simplified model for (a) compensation current i_{fa} and (b) dc capacitor voltage v_{dc} .

3.6.3 DSTATCOM Operating in Voltage Mode

The basic purpose of the DSTATCOM is to compensate the load injecting currents in such a way that at the point of common coupling (PCC) the source current and the PCC voltage are balanced and sinusoidal. In practice, however, the loads are remote from the distribution substations and are supplied by feeders. Under this situation, the source is termed as non-stiff. The reference compensator currents generated by these shunt algorithms are tracked using a voltage source converter (VSC) in the hysteresis scheme. As a consequence of this, the compensated source currents contain the inverter switching frequency components. This will result on distorted terminal voltages at the PCC due to the feeder impedance. Now, these distorted PCC voltages are taken as input voltage signals by shunt algorithms, which generally assume a balanced voltage supply. Therefore, the control algorithms generate erroneous reference filter currents and consequently the source currents are also distorted. Thus, it is easy to infer that the direct application of these shunt

algorithms with non-stiff source results on distorted PCC voltages and severely distorted source currents. In this thesis, the control strategy proposed in [Mishra, et al. 2003] is used. With this algorithm, the DSTATCOM operates as a voltage regulator to maintain constant the voltage of a specified bus (PCC). The magnitude of the bus voltage is pre-specified, while its phase angle is generated from a dc capacitor control loop. A deadbeat controller for the inverter is used for voltage tracking. With this algorithm, the DSTATCOM can compensate the terminal voltage, irrespective of any distortion or unbalance in the load or in the voltage source. For more details about this algorithm, please refer to [Mishra, et al. 2003].

3.6.3.1 Simplified DSTATCOM Model

In the simplified model, the three H-bridge converters are replaced by three controllable voltage sources. The main advantage of this model is to allow larger integration steps. Besides, the limit cycle can be computed using a shooting method and its stability can be directly assessed through the eigenvalues of the Jacobian of the Poincaré map, which are the Floquet multipliers. Moreover, this model is suitable for dynamic studies using instantaneous or phasor variables for the network representation, if the harmonic distortion is not taken into account. In Figure 3.26, the schematic representation for the simplified model of DSTATCOM operating in voltage mode is shown. This model is based on the assumption that $v_{tx} = v_{tx}^*$, where v_{tx}^* is the reference terminal voltage. Figure 3.27 shows the schematic representation of the dc link model.

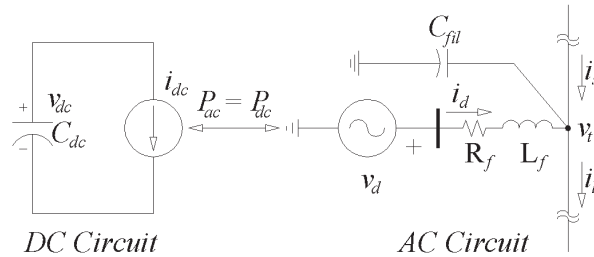


Figure 3.26 Schematic representation for the simplified model.

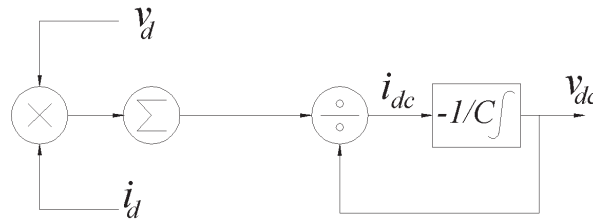


Figure 3.27 dc link model.

The reference terminal voltage v_{tx}^* is

$$v_{tx}^* = V_m \sin(\omega t - \delta - \varphi_x) \quad (3.42)$$

and δ is computed using a proportional-integral controller described by,

$$\delta = K_{p\delta} (P_{sh} - P_{sh}^*) + K_{i\delta} \int (P_{sh} - P_{sh}^*) dt \quad (3.43)$$

P_{sh} is the instantaneous power reference in the shunt link and P_{sh}^* is its reference; P_{sh} is given by

$$P_{sh} = v_{ta} i_{fa} + v_{tb} i_{fb} + v_{tc} i_{fc} \quad (3.44)$$

P_{sh}^* is obtained as,

$$P_{sh}^* = K_{pdc} (v_{dc}^{average} - v_{dc}^*) + K_{idc} \int (v_{dc}^{average} - v_{dc}^*) dt \quad (3.45)$$

where v_{dc}^* is the reference dc voltage, $v_{dc}^{average}$ is the average voltage across the dc capacitor. The converter terminal voltage is given by,

$$v_{dx} = R_f i_{dx} + L_f \frac{di_{dx}}{dt} + v_{tx} \quad (3.46)$$

The current injected by the compensator is calculated by,

$$i_{dx} = -C_{fil} V_m \sin(\omega t - \delta - \phi_x) \left(\omega - \frac{d\delta}{dt} \right) + i_{lx} - i_{sx} \quad (3.47)$$

The first derivative of i_{dx} is computed as,

$$\frac{di_{dx}}{dt} = \frac{d(i_{lx} - i_{sx})}{dt} - C_{fil} V_m \left(\sin(\omega t - \delta - \phi_x) \frac{d^2\delta}{dt^2} + \cos(\omega t - \delta - \phi_x) \left(\omega - \frac{d\delta}{dt} \right)^2 \right) \quad (3.48)$$

The dynamic capacitor voltage is given by,

$$C_{dc} \frac{dv_{dc}}{dt} = -\frac{i_{da} v_{da} + i_{db} v_{db} + i_{dc} v_{dc}}{v_{dc}} \quad (3.49)$$

where

$$x = a, b, c$$

$$\varphi_a = 0; \varphi_b = 2\pi/3; \varphi_c = -2\pi/3$$

$$\frac{d\delta}{dt} = K_{p\delta} \left(\frac{dP_{sh}}{dt} - K_{pv} \frac{dv_{dc}^{average}}{dt} \right) + K_{i\delta} (P_{sh} - P_{sh}^*) \quad (3.50)$$

$$\frac{d^2\delta}{dt^2} = K_{p\delta} \left(\frac{d^2 P_{sh}}{dt^2} - K_{pv} \frac{d^2 v_{dc}^{average}}{dt^2} \right) + K_{i\delta} \left(\frac{dP_{sh}}{dt} - K_{pv} \frac{dv_{dc}^{average}}{dt} \right) \quad (3.51)$$

In comparison to the detailed model, the simplified model is advantageous, since the simplified models can be described only with an ODEs set. In addition, the simplified model can achieve a higher precision than the detailed model as shown in Figure 3.24, for the same integration steps. There are some disadvantages with the simplified DSTATCOM model. Basically, the high frequency phenomena are neglected. However, to avoid erroneous interpretations in our bifurcation analysis, the bifurcation diagrams are validated against time domain simulation carried-out with the detailed model implemented in Simulink.

3.6.3.2 Comparative Analysis of Models for the DSTATCOM in Voltage Mode

In this section, the performance of the simplified DSTATCOM model is compared against the detailed model. The system parameters and the DSTATCOM parameters for the circuit shown in Figure 3.21 are given in Table 3.2. The hysteresis band for the detailed model is $h=10$.

TABLE 3.2 SYSTEM PARAMETERS OF THE DSTATCOM IN VOLTAGE MODE

Systems Parameters	DSTATCOM Voltage Mode
System voltage (V_s): 440 V (peak), sinusoidal and may contain harmonics, exhibit sags and swells, and possible unbalance.	Voltage controllers gains of dc capacitor loops: $K_{pdc}=154, K_{idc}=3500$.
Feeder impedance (R_s, L_s): $1+j 7.54 \Omega$	δ control loop gains: $K_{p\delta}=27e-6, K_{i\delta}=8e-3$.
ac capacitor (C_{ac}): 70 μ F	dc capacitor (C_{dc}): 1500 μ F
Feeder load impedance (R_l, L_l): $0.5+j 3.77 \Omega$	Interface circuits (R_f, L_f): $0.05+ j 3.77 \Omega$
EAF constants: $K_1=15, K_2=0.05, K_3=800, m=0$ and $n=2$.	Reference value of dc capacitor voltage: 1200 V

Initially, the electric system is in periodic steady state and the switch sw is open. At $t=0$ s, the switch sw is closed, thus, the DSTATCOM starts to regulate the terminal voltage v_t at the PCC bus. Figure 3.28(a) shows the results comparison for the phase angle δ , Figure 3.28(b) shows the comparison for the voltage across the dc capacitor v_{dc} , and Figure 3.28(c) for the compensation current i_{fa} . The results show a very good agreement between the simplified model and the detailed model, with an integration step size of 60 μ s and 1 μ s, respectively. An excellent agreement between the two models is achieved, even though the simplified model has a considerably larger integration step (60 times). The detailed model needs to use a small integration step to avoid the numerical error introduced by the commutation process.

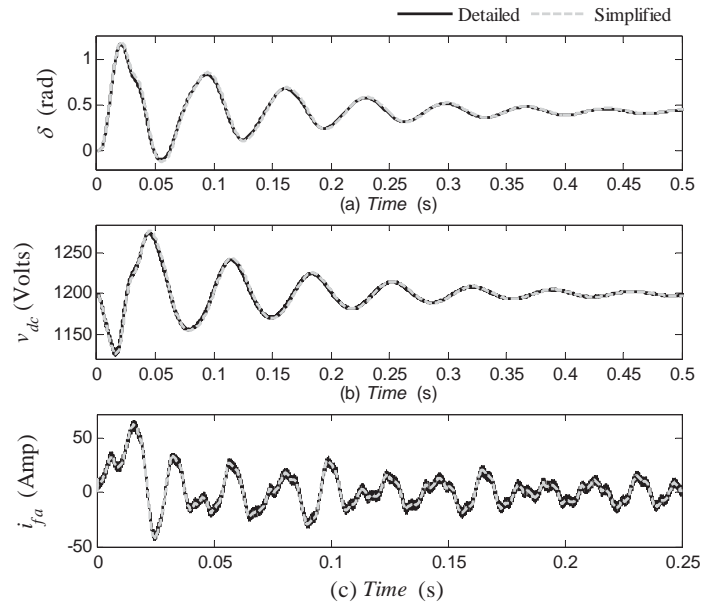


Figure 3.28 Comparison in the time domain between the detailed and the simplified model for (a) phase angle δ , (b) dc capacitor voltage v_{dc} , and (c) compensation current i_{fa} .

A strong correlation between the detailed model and the simplified model results is further illustrated in Figure 3.29, which shows the harmonic spectrum for the compensation current i_{fa} .

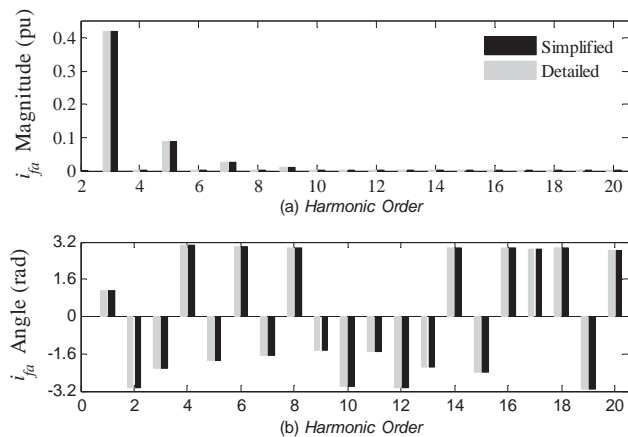


Figure 3.29 Spectrum comparison between the detailed and the simplified model for i_{fa} .

3.7 Ideal Source and Smooth Hysteresis Band Approach: Comparative Analysis

3.7.1 DSTATCOM Operating in Current Mode

A comparison between the detailed model and the simplified model based on the ideal source approach is shown in Figure 3.30. The compensator current i_{fa} , the terminal voltage

v_{ta} , and the dc voltage capacitor v_{dc} , are shown in Figure 3.30(a), Figure 3.30(b), and Figure 3.30(c), respectively.

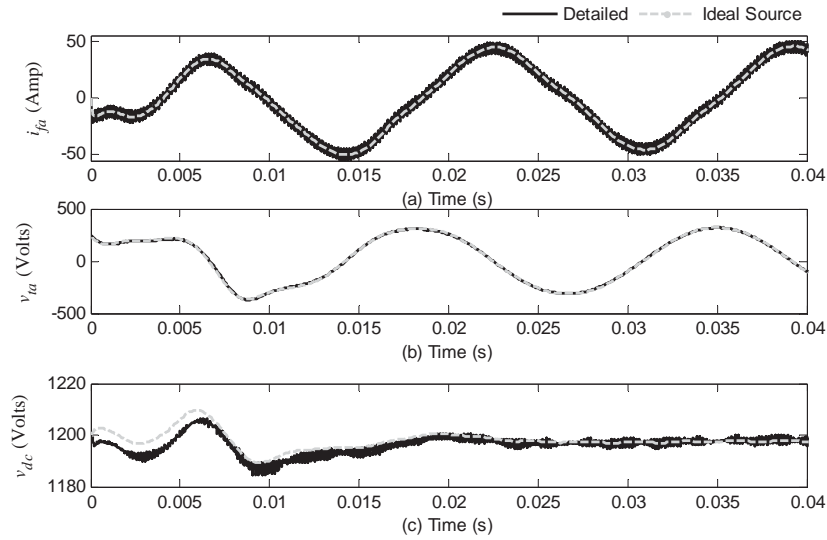


Figure 3.30 Comparison in the time domain between the detailed and the simplified model based on the ideal source approach for (a) compensation current i_{fa} , (b) terminal voltage v_{ta} , and (c) dc capacitor voltage v_{dc} .

The same comparison for the simplified model based on the hyperbolic tangent approach is presented in Figure 3.31. For this numerical experiment, the hysteresis band has been selected as $h=5$ A. Observe that the dc voltage capacitor computed with the ideal current source models has a small error. This error is because this model assumes that the DSTATCOM generates the compensation currents instantaneously. On the other hand, the model based on the hyperbolic tangent gives much better solutions since it is not assumed that the compensator generates the compensation currents instantaneously.

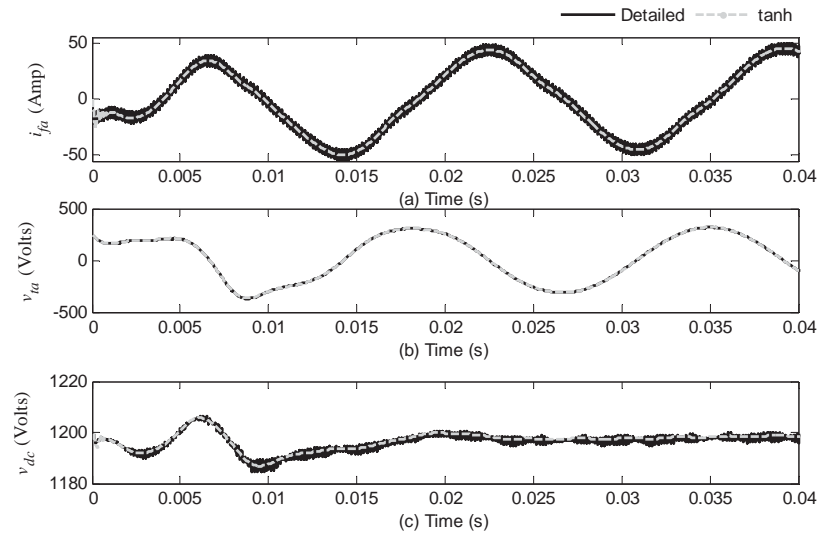


Figure 3.31 Comparison in the time domain between the detailed and the simplified model based on the ideal source approach for (a) compensation current i_{fa} , (b) terminal voltage v_{ta} , and (c) dc capacitor voltage v_{dc} .

3.7.2 DSTATCOM Operating in Voltage Mode

The comparison solution for the DSTATCOM operating in voltage mode for the phase angle δ , the dc capacitor voltage v_{dc} , and the terminal voltage v_{tc} are presented in the Figure 3.32(a), Figure 3.32(c), and Figure 3.32(e), respectively. Observe from Figure 3.32(b), Figure 3.32(d), and Figure 3.32(f) that for this particular case, the solution obtained with the simplified model based on ideal voltage sources does not give an accurate solution during the first cycles for these variables.

The same comparison for the simplified model based on the hyperbolic tangent is presented in Figure 3.33. Please notice that the initial transients can be accurately reproduced with the simplified model based on this approach.

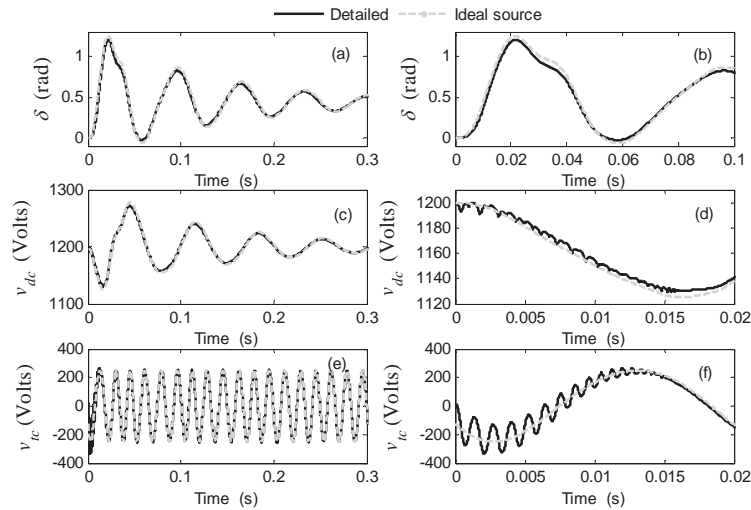


Figure 3.32 Comparison in the time domain between the detailed and the simplified based on the ideal source approach for (a) phase angle δ , (b) phase angle δ during the first 0.02 s, (c) dc capacitor voltage v_{dc} , (d) dc capacitor voltage v_{dc} during the first 0.02 s, (e) terminal voltage v_{tc} , (f) terminal voltage v_{tc} during the first 0.02 s.

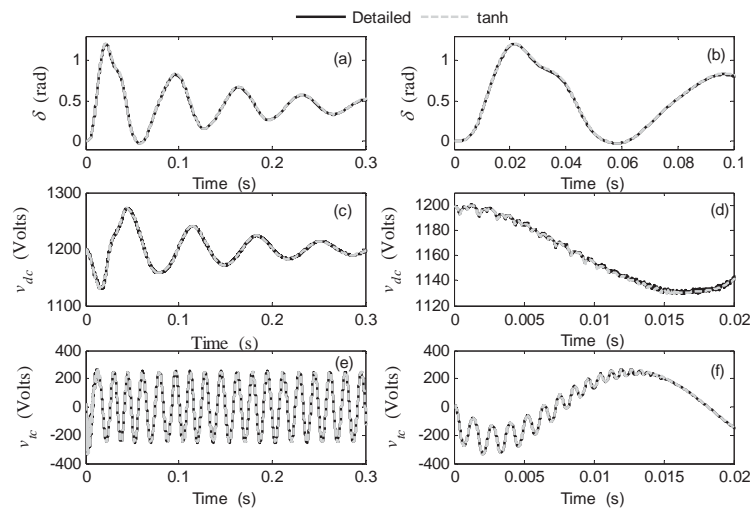


Figure 3.33 Comparison in the time domain between the detailed and the simplified based on the sigmoid function approach for (a) phase angle δ , (b) phase angle δ during the first 0.02 s, (c) dc capacitor voltage v_{dc} , (d) dc capacitor voltage v_{dc} during the first 0.02 s, (e) terminal voltage v_{tc} , (f) terminal voltage v_{tc} during the first 0.02 s.

3.8 Dynamic Voltage Restorer

The capacitor-supported DVR is a power electronic converter-based device that has been proposed to protect critical and sensitive loads from supply-side disturbances, except outages [Ghosh and Ledwich 2002]. It is connected in series with a distribution feeder and it is capable of generating or absorbing real and reactive power at its ac terminals. The operation principle of the DVR is simple; it injects a voltage in series with the feeder. Ideally, this injected voltage is in quadrature with the line current so that the DVR behaves like an inductor or a capacitor for the purpose of increasing or reducing the overall reactive voltage drop across the feeder. In this operating mode, the DVR does not have any interchange of real power with the system in steady-state. The DVR can restore the load-side voltage to the desired amplitude and waveform even when the source voltage is unbalanced and distorted. The DVR is based on a voltage source converter. The output of the VSC is connected in series with a distribution feeder through a transformer. This device use IGBTs that are operated in a PWM fashion. The VSC is supplied by a dc capacitor. A schematic representation of the DVR is shown in Figure 3.34.

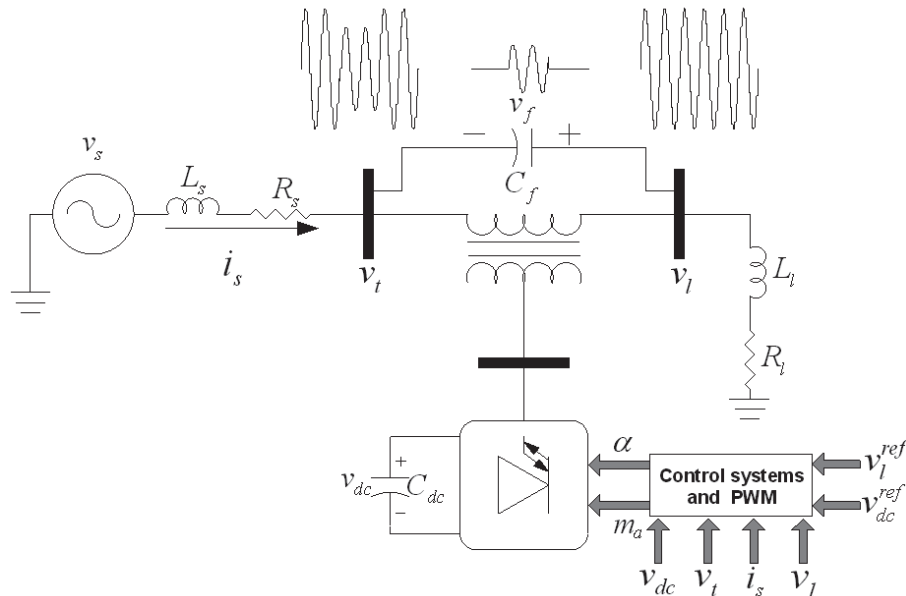


Figure 3.34 DVR inserting voltage to protect a sensitive load.

3.8.1 DVR Reference Voltage Generation

The compensation algorithm for the DVR here used is based on that proposed in [Ghosh and Ledwich 2002]. The schematic diagram of a series compensated distribution system is shown in Figure 3.34. The DVR is connected in series between the PCC and the load. The DVR is represented by the voltage sources v_{fa} , v_{fb} , and v_{fc} ; the supply voltages are v_{sa} , v_{sb} , and v_{sc} ; the load voltages are v_{la} , v_{lb} , and v_{lc} ; the terminal voltages at the PCC bus are represented v_{ta} , v_{tb} , and v_{tc} ; and the line currents are represented by i_{sa} , i_{sb} , and i_{sc} . The critical load is represented by the impedances Z_{la} , Z_{lb} , and Z_{lc} .

The subscripts a , b , and c denote the phases. However, in the following analysis, these are omitted and any equation applies to all three phases. The source is connected to the

DVR through a feeder with an impedance of $R_s + jX_s$. The uppercase characters represent phasor quantities.

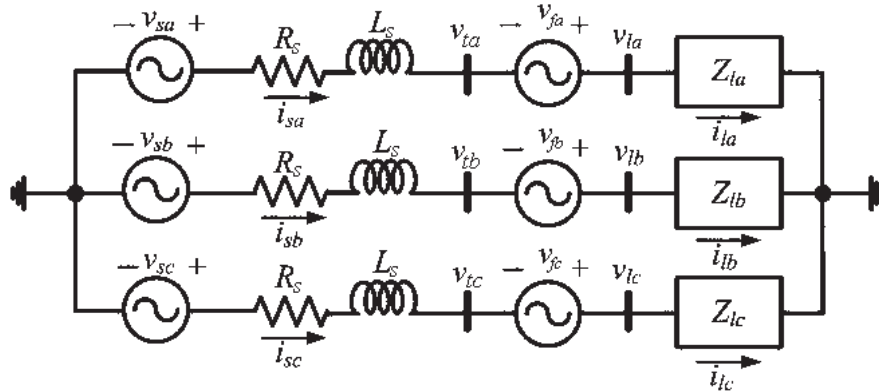


Figure 3.35 Schematic diagram of a distribution system with ideal series compensator.

With respect to Figure 3.35, using KVL at PCC bus and neglecting the impedance of the DVR injection transformer, we get

$$\mathbf{V}_t = \mathbf{V}_i + \mathbf{V}_f \quad (3.52)$$

To avoid the interchange of real power in steady-state between the DVR and the network, \mathbf{V}_f must be in quadrature with the line current \mathbf{I}_s . Let's denote the phasor source current as $\mathbf{I}_s = |\mathbf{I}_s| \angle \theta$, where $|\mathbf{I}_s|$ is the magnitude of \mathbf{I}_s , and θ is its angle. \mathbf{I}_s is obtained from measurements. Therefore, \mathbf{V}_f is defined by,

$$\mathbf{V}_f = |\mathbf{V}_f| \angle \theta + \pi / 2 \quad (3.53)$$

Equation (3.53) can be represented in rectangular form as,

$$\mathbf{V}_f = |\mathbf{V}_f| (a_1 + jb_1) \quad (3.54)$$

The terminal voltage \mathbf{V}_t can be expressed as,

$$\mathbf{V}_t = |\mathbf{V}_t| (a_t + jb_t) \quad (3.55)$$

From (3.52), (3.54) and (3.55), we get,

$$|\mathbf{V}_f|^2 + 2|\mathbf{V}_t|(a_t a_1 + b_t b_1)|\mathbf{V}_f| + |\mathbf{V}_t|^2 - |\mathbf{V}_i|^2 = 0 \quad (3.56)$$

Equation (3.56) has two solutions, given by

$$|\mathbf{V}_f| = \frac{-b \pm \sqrt{b^2 - 4c}}{2} \quad (3.57)$$

where,

$$b = 2|V_t|(a_1 a_1 + b_1 b_1) \quad (3.58)$$

$$c = |V_t|^2 - |V_l|^2 \quad (3.59)$$

Negative and complex values of $|V_f|$ are not feasible. The solution that must be chosen from (3.57) is the real and positive, when a solution exists.

3.8.2 DVR Structure

Figure 3.36 shows the DVR structure in which a filter capacitor C_f is connected in parallel with the DVR. The voltage v_f is the voltage across the filter capacitor C_f [Ghosh and Jindal 2004].

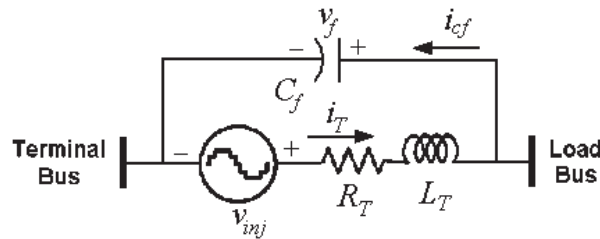


Figure 3.36 Single-phase equivalent circuit of the DVR with filter capacitor connected in shunt with the DVR.

The converters shown in Figure 2.12, Figure 2.15, and Figure 2.21, among other, can be used for the DVR purposes.

In Figure 3.36, v_{inj} is the voltage at the converter terminals - this voltage is represented in terms of the switching functions.

3.8.3 Closed-Loop Compensation Algorithm

The compensation formula given by (3.57) gives the magnitude of the voltage that must be injected in series by an ideal DVR (no voltage drop across the injection transformer) to compensate the magnitude of the voltage at the load bus. We can see (3.57) as an open-loop compensation algorithm. However, for a real case, there is a voltage drop across the injection transformer. Therefore, an open-loop compensation algorithm is not suitable to compute the voltage that must be injected by the DVR, and a feedback compensation algorithm is needed instead. For this case, a PI controller is used; this is given by

$$|V^{ref}| = K_{vp} (|V_l^{ref}| - |V_l|) + K_{vi} \int (|V_l^{ref}| - |V_l|) dt \quad (3.60)$$

where $|V_l^{ref}|$ is the load voltage reference magnitude, $|V_l|$ is the load voltage magnitude, obtained from measurements. Thus, the closed-loop compensation algorithm is given by

$$|V_{inj}|^2 + 2|V_t|(a_t a_1 + b_t b_1)|V_{inj}| + |V_t|^2 - |V^{ref}|^2 = 0 \quad (3.61)$$

A feasible solution of (3.61) is

$$|V_{inj}| = \min \left(\frac{-b \pm \sqrt{b^2 - 4c}}{2} \right) \quad (3.62)$$

where

$$b = 2|V_t|(a_t a_1 + b_t b_1) \quad (3.63)$$

$$c = |V_t|^2 - |V^{ref}|^2 \quad (3.64)$$

Figure 3.37 illustrates the DVR control system, where m_a is the amplitude modulation ratio and α is the phase of the voltage control signal at the converter terminal.

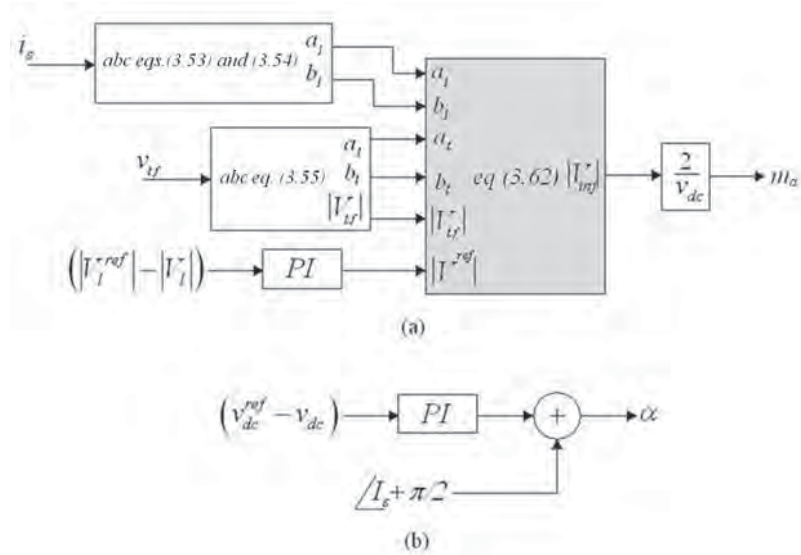


Figure 3.37 Circuit control of the DVR.

The performance of the DVR directly depends on its control system; however, there are some limitations that are not associated with the control systems but with the compensation limits of the DVR. These compensation limits are given by the solutions of (3.61); if there is not a real and positive solution means that the DVR is out of its compensation limits, which imply that no matter what compensation algorithm, control system, or gains set are used, the DVR will not properly compensate.

3.8.4 Test Case

Let consider the electric system shown in Figure 3.34. For this particular case, the control system used for the DVR is that shown in Figure 3.37; however another control

system can be used. The set of parameters are given in Table 3.3. The modulation frequency ratio for this case is 27.

In the simulation experiment, the load voltage is regulating at $v_l = 1$ pu. At $t = 0.05$ s the source voltage is changed from 1 pu to 1.45 pu. Observe in Figure 3.38(a) that the terminal voltage varies as the source voltage varies; however, the load voltage shown in Figure 3.38(b) is kept constant at 1 pu. The compensation voltage v_f is shown in Figure 3.38(c). Please observe in Figure 3.38(c) that during the swell the DVR reduces the injected voltage to maintain the load voltage at its reference value.

TABLE 3.3 SYSTEM PARAMETERS OF THE DVR

Systems Parameters	DVR
System voltage ($ V_s $): 1 pu	Voltage controllers gains of dc capacitor loops: $K_{pdc}=1, K_{idc}=0.5$.
Feeder impedance (R_s, X_s): $0.05+j 0.94$ pu	V_l control loop gains: $K_{pv}=0.05, K_{iv}=180$.
ac capacitor reactance (X_{ac}): 17.6 pu	dc capacitor reactance (X_{dc}): 8.84 pu
Load impedance (R_l, L_l): $2+j 1.8$ pu	Injection transformer impedance (R_T, L_T): $0.02+j 0.19$ pu

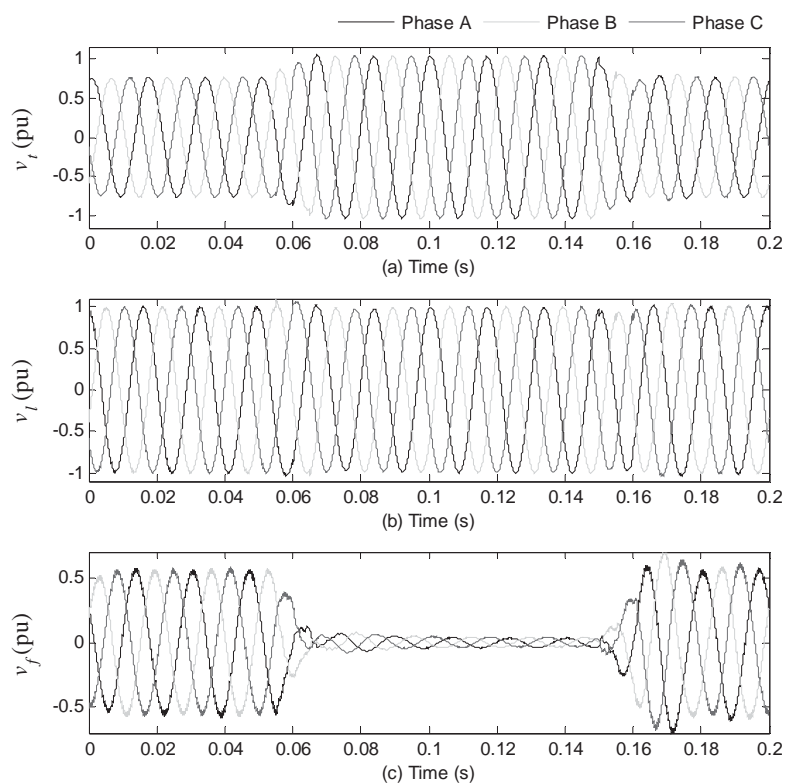


Figure 3.38 Transient solutions for the operation of the DVR. (a) Terminal voltage, (b) Load voltage, and (c) Compensation voltage.

3.8.5 Experimental Verification of the Fourier and Hyperbolic models

In this section laboratory results of an Adjustable Speed Drive (ASD) are presented in order to demonstrate the reliability of the proposed models for the VSCs. This experiment is focused on scalar-based speed controllers which are known as constant V/H control [Bose 2002]. The electric network including the ASD is modeled in abc and the induction machine in the dqo rotating frame of reference.

3.8.5.1 State Space Representation

The ASD structure used in our analysis is shown in Figure 3.39. It contains a diode-bridge and a voltage-source inverter (VSI) operated in a pulse width modulation fashion connected to a common dc-link. This circuits constitute a nonlinear periodically excited system with a T - periodic function, which can be represented by the following nonlinear system:

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, t; \mathbf{M}) \quad (3.65)$$

Where \mathbf{x} and \mathbf{f} are n - dimensional vectors, and \mathbf{M} is an m - dimensional parameter vector. In particular, for the electric circuit shown in Figure 3.39, the ODE set is defined as

$$\frac{d}{dt} \begin{bmatrix} i_s \\ v_{dc} \\ F_{qs} \\ F_{ds} \\ F_{qr} \\ F_{dr} \\ \omega_r \end{bmatrix} = \begin{bmatrix} -\frac{(R_s + r)}{L_s} i_s - \frac{v_t}{L_s} + \frac{v_s}{L_s} \\ (i_r - i_L) / C_{dc} \\ \omega_b \left[v_{qs} - \omega_e / \omega_b \lambda_{ds} + \frac{R_s}{X_{ls}} \left(\frac{x_{ml}^*}{x_{lr}} \lambda_{qr} + \left(\frac{x_{ml}^*}{x_{ls}} - 1 \right) \lambda_{qs} \right) \right] \\ \omega_b \left[v_{ds} + \omega_e / \omega_b \lambda_{qs} + \frac{R_s}{X_{ls}} \left(\frac{x_{ml}^*}{x_{lr}} \lambda_{dr} + \left(\frac{x_{ml}^*}{x_{ls}} - 1 \right) \lambda_{ds} \right) \right] \\ \omega_b \left[-\frac{(\omega_e - \omega_r)}{\omega_b} \lambda_{dr} + \frac{R_r}{x_{lr}} \left(\frac{x_{ml}^*}{x_{ls}} \lambda_{qs} + \left(\frac{x_{ml}^*}{x_{lr}} - 1 \right) \lambda_{qr} \right) \right] \\ \omega_b \left[\frac{(\omega_e - \omega_r)}{\omega_b} \lambda_{qr} + \frac{R_r}{x_{lr}} \left(\frac{x_{ml}^*}{x_{ls}} \lambda_{ds} + \left(\frac{x_{ml}^*}{x_{lr}} - 1 \right) \lambda_{dr} \right) \right] \\ \frac{p}{2J} (T_e - T_L) \end{bmatrix} \quad (3.66)$$

with

$$X_{ml}^* : 1 / \left(\frac{1}{x_m} + \frac{1}{x_{ls}} + \frac{1}{x_{lr}} \right) \quad (3.67)$$

$$T_e = 0.75p(\lambda_{ds}i_{qs} - \lambda_{qs}i_{ds}) / \omega_b \quad (3.68)$$

$$v_t = \begin{bmatrix} S_{Ba} - \frac{1}{3} \sum_{i=a,b,c} S_{Bi} \\ S_{Bb} - \frac{1}{3} \sum_{i=a,b,c} S_{Bi} \\ S_{Bc} - \frac{1}{3} \sum_{i=a,b,c} S_{Bi} \end{bmatrix} v_{dc} \quad (3.69)$$

$$i_r = \sum_{i=a,b,c} i_{si} S_{Bi} \quad (3.70)$$

$$i_L = \sum_{i=a,b,c} i_{Mi} S_i \quad (3.70)$$

For a squirrel cage induction machine as is the case of this study, v_{qr} and v_{dr} are zero. S_{Bi} and S_i (for $i=a,b,c$) are the switching functions for the diode-bridge rectifier and the voltage source inverter (VSI), respectively. The behavior of the system is represented by a set of 9 ODEs.

3.8.5.2 Simulated and Experimental Results

In this section, the laboratory results are presented in order to show the performance of the proposed models. A simplified distribution system shown in Figure 3.39 is assumed, in which a three-phase load is supplied by a source through a radial feeder. The experimental parameters are given in Table 3.4 and Table 3.5.

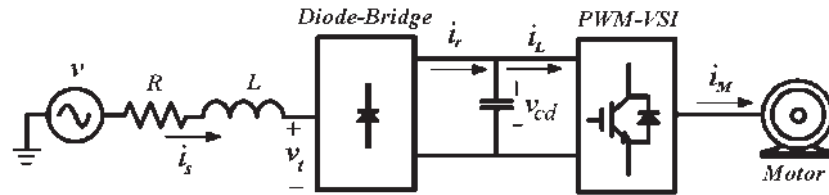


Figure 3.39 Experimental system configuration.

TABLE 3.4 INDUCTION MOTOR PARAMETERS

Rotor Resistance:	12 Ω
Stator Resistance:	12 Ω
Stator Inductance:	0.018 H
Rotor Inductance:	0.018 H
Magnetizing Inductance:	0.16 H
Rotor viscous friction coefficient:	0.0005
Number of Poles:	4
Rotor inertia coefficient:	0.015 kg m ²
Mechanical load torque:	0 N-m

TABLE 3.5 SYSTEM PARAMETERS

System voltage (v): 216.7 Volts (L-L rms).
Feeder impedance (R, L): $0.1+j 0.0136 \Omega$
DC capacitor(C_{dc}): 1100 μF

Figure 3.40 and Figure 3.41 show the simulated and experimental waveforms in steady state, respectively. The simulated results have been obtained using the Fourier approach and the hyperbolic tangent model. Observe that these results are in good agreement in comparison with the experimental results.

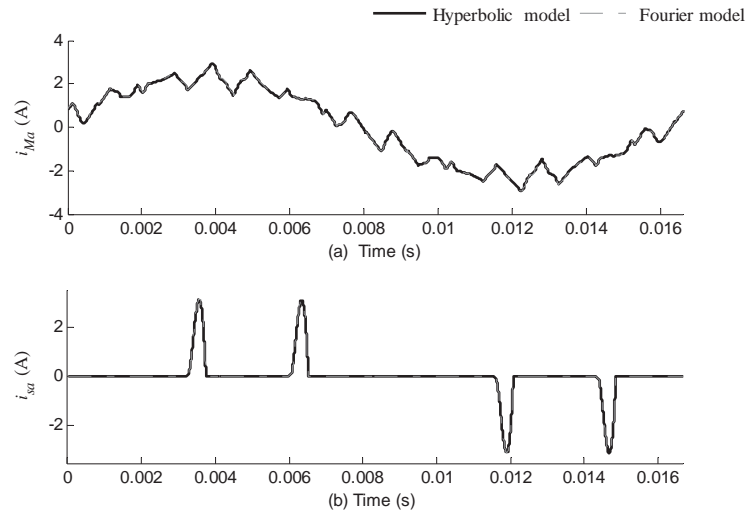


Figure 3.40 Simulated waveforms (a) Motor current of phase A (b) Rectifier current of phase A.

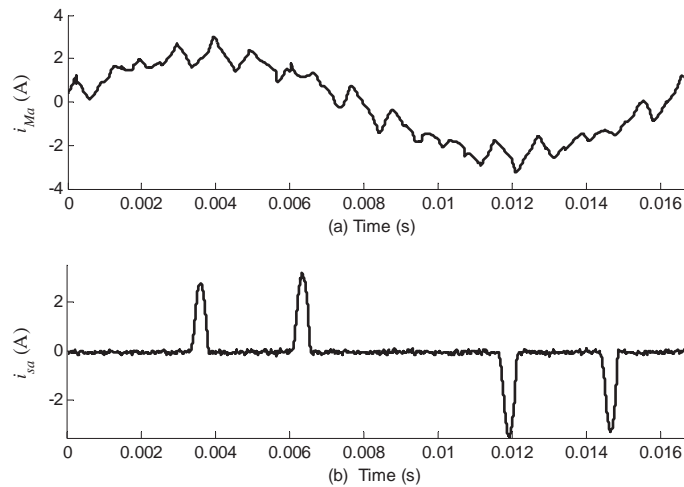


Figure 3.41 Experimental waveforms (a) Motor current of phase A (b) Rectifier current of phase A.

A validation of the proposed models is further illustrated in Figure 3.42 and Figure 3.43. The harmonic spectrum for the motor current of phase A is presented in Figure 3.42(a) and Figure 3.43(a), respectively. The harmonic spectrum for the inverter current of phase A is

presented in Figure 3.42(b) and Figure 3.43(b), respectively. Observe that all the solutions are in excellent agreement.

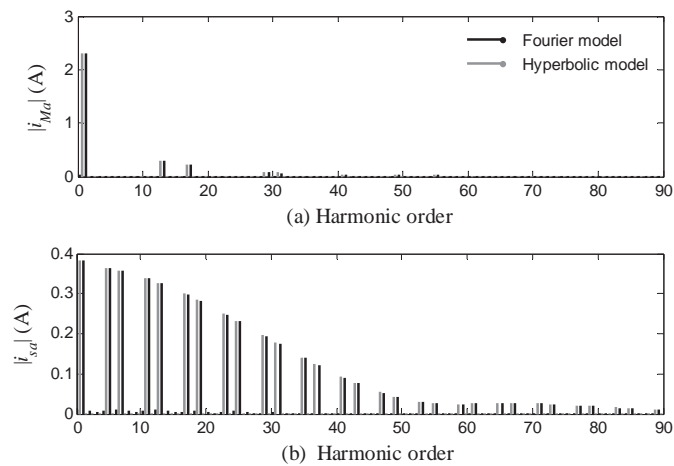


Figure 3.42 Harmonic content computed with proposed models. (a) Harmonic content in the motor current of phase A. (b) content in the rectifier current of phase A.

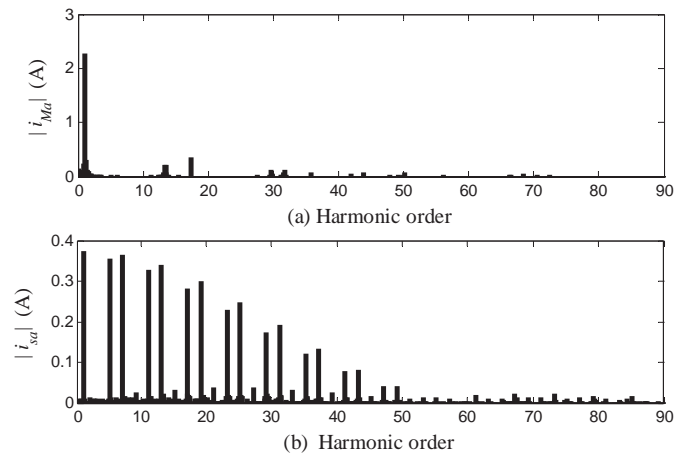


Figure 3.43 Harmonic content obtained from measurements. (a) Harmonic content in the motor current of phase A. (b) content in the rectifier current of phase A.

The difference between the simulation and experimental results is due to the following reasons:

1. The hyperbolic tangent model and the Fourier model do not take into account the forward voltage of the IGBT, the snubber circuit, and the switching on and off times.
2. The harmonics in the network are not taken into account.
3. The voltage oscillation in the voltage source is not taken account.

The formal basis and dynamic behavior of the ASD using the proposed models have been presented. Besides, a circuit implemented in the laboratory has been used to validate these models and the results compared well with those obtained by simulation. As a result

of these comparisons, it can be concluded that the proposed model works very well and is well suited for time domain simulation of any device based on SPWM VSCs.

3.9 Conclusions

Two efficient Voltage Source Converter models based on a Fourier series approach and a hyperbolic tangent procedure have been proposed for the six-pulse converter. The proposed models have been used for the computation of the solution of FACTS devices connected to a power network.

It has been shown that the proposed models can be used to compute both the transient and the periodic steady state solution of a power network containing VSC-based FACTS.

The response given by the proposed methods has been successfully validated against the solution obtained with the widely accepted digital simulators Simulink and PSCAD/EMTDC, respectively. In all cases the obtained results were in excellent agreement. In addition, it has been shown through simulations that the proposed models allow larger integration steps, as compared with the ideal switch model approach, e.g. for the conducted studies, more than 800 times the integration step needed by Simulink and PSCAD/EMTDC when the Fourier approach was used, and at least 300 times when the hyperbolic tangent method was applied.

The proposed VSCs models have been only implemented in a network including FACTS devices; however, these models can be used in any power electronic device based on SPWM six pulse converters, or even for multilevel converters based on arrangement of six-pulse converters.

Two different state space approaches have been used to represent in the time domain the dynamics of the DSTATCOM connected to the system. Particularly, the models based on the sigmoid or hyperbolic tangent model can be used for representing the switching functions in the hysteresis band modulation technique of any other device, for example, the DVR, and the UPQC, among others.

An experimental validation of the proposed VSC based on the Fourier approach and the hyperbolic tangent model has been provided in order to demonstrate the applicability of these mathematical models.

In [Segundo-Ramírez and Medina 2009] a Newton method and the proposed VSCs-based models on the Fourier and hyperbolic tangent techniques have been applied to compute the periodic steady state solution of power network including FACTS devices. In that article, the power restrictions have been imposed using PI controllers; however, the dynamics equations of the PI controllers can be transformed into algebraic restrictions if the integral gains are fixed equal to zero. Thus, this periodic steady state solution [Segundo-Ramírez and Medina 2009] is a harmonic power flow in the time domain of power networks including FACTS devices.

4 Construction of Periodic Solutions

This Chapter describes on detail of the development of Newton methods based on an Enhanced Numerical Differentiation method (END) and Discrete Exponential Expansion (DEE) procedures, respectively, for the fast and efficient computation of the periodic steady state solution of nonlinear power systems. These methods are used to compute the periodic steady-state of nonlinear switched circuits

4.1 Introduction

The periodic steady-state solution of an electric/electronic system is required for different types of studies. For instance, it is needed in electronic circuits since the circuit design specifications are given for its period steady-state operation. In power quality analysis, the periodic steady-state solution is needed to assess the network harmonic content. The computation of bifurcation diagrams through continuation methods requires the efficient computation of the periodic steady-state solution; in addition, information concerning the stability of the detected limit cycle is needed [Parker and Chua 1989]. Other practical application is for the initialization of simulation software of the EMTP type for electromagnetic transient [Perkins, et al. 1995] [Wang and Marti 1996] [Neves, et al. 2006].

The practical precision required for the periodic steady-state solution depends on the analysis to be done, e.g. a precision of 10^{-5} is sufficient to quantify the harmonic distortion in power networks, to initialize EMTP-type programs and for the determination of practical specification of electronic circuits. However, more rigorous and precise steady-state solutions are essential for the determination of bifurcation diagrams [Parker and Chua 1989].

The methods to compute the periodic steady state solution may be grouped in two distinct classes, e.g. according to the fact of being based on a time-domain and on a frequency domain approach, respectively. The former can be considered as derivations or improvements of the shooting method [Aprille Jr. and Trick 1972] and the latter as derivations of the harmonic balance method [Lindenlaub 1969]. In this thesis, we consider only the time domain methods.

Established knowledge on the modeling and analysis of power systems indicates that the periodic steady-state solution of nonlinear power networks can be obtained in the time domain through the direct application of a numerical integration method to solve the resulting system, representing the dynamic behavior of the electric network, once the

transient eventually dies-out [Parker and Chua 1989]. However, the application of this Brute Force approach (BF) can take an excessive computational effort in poorly damped systems. This drawback has limited the application of the time domain for the computation of the periodic steady state solution of nonlinear systems, especially if these are poorly damped. Besides, the BF method has notorious difficulties to locate unstable limit cycles [Parker and Chua 1989]. To overcome this problem, an early contribution [Aprille Jr. and Trick 1972] proposed a Newton method in the time domain for the fast periodic steady state solution of nonlinear circuits, namely the shooting method. In [Colon and Trick 1973] and [Grosz and Trick 1982], some modifications to the Newton method are proposed to improve the convergence of the Newton method presented by Aprille and Trick. In [Colon and Trick 1973] a method is presented based on finite differences to obtain the Jacobian of the Poincaré map (Φ). In addition, it has been shown in [Colon and Trick 1973] that the shooting method can be added to most current transient circuit analysis programs, in order to provide fast steady state analysis of large-signal circuits. In [Perkins, et al. 1995], [Wang and Marti 1996], and [Neves, et al. 2006] different procedures are proposed for the computation of the steady-state to initialize EMTP-type programs. In contributions [Usaola-Garcia 1990] and [Semlyen and Medina 1995] Newton methods are used to solve in the time domain the nonlinear networks of a hybrid time and frequency representation of power systems. In [Usaola-Garcia 1990] the shooting method reported in [Aprille Jr. and Trick 1972] is used and in [Semlyen and Medina 1995] three different Newton type procedures are proposed to obtain Φ . In [Bedrosian and Vlach 1992], [Donde and Hiskens 2006], [Garcia and Medina 2003], [Medina, et al. 2003], [Chang, et al. 2006], [Lizhong and Vlach 1995], [Armanazi 1973], [Wong 1987], [Kuroe, et al. 1988], and [Li and Tymerski 2000] Newton methods are applied to obtain the periodic steady state solution of systems containing commutated devices. In [Li and Tymerski 2000] a comparison of the different algorithms for the accelerated determination of periodic steady state of switched networks is presented.

The Newton methods require the computation of the state transition matrix to be used during the iterative solution process. An important part of these Newton techniques is the process followed to obtain Φ . Different procedures have been proposed to obtain Φ ; [Aprille Jr. and Trick 1972], [Colon and Trick 1973], [Semlyen and Medina 1995], and [Li and Tymerski 2000].

4.2 Fast Time Domain Solution

Let us assume the following nonlinear time-varying system periodically excited with a T -periodic function,

$$\dot{\mathbf{x}}(t) = \mathbf{f}(t, \mathbf{x}), \quad \mathbf{x}(t_0) = \mathbf{x}_0 \quad (4.1)$$

where \mathbf{x} and \mathbf{f} are n -dimensional vectors, $\mathbf{f}(t, \mathbf{x})$ is piecewise continuous and has a continuous first derivative with respect to \mathbf{x} . We assume that $\mathbf{f}(t, \mathbf{x})$ is T -periodic, so $\mathbf{f}(t, \cdot) = \mathbf{f}(t+T, \cdot)$. Also, it is assumed that the trajectory started in \mathbf{x}_0 is attracted to a limit cycle of period T , so (4.1) has a periodic steady state solution $\varphi(t+T) = \varphi(t)$, where φ is the orbit of the system (4.1) in the limit cycle. Since the solution of (4.1) is assumed periodic, it can be found by using the Poincaré map to extrapolate the state variables to the limit cycle

through the application of a Newton method. The state variables \mathbf{x}^∞ at the limit cycle are estimated as [Semlyen and Medina 1995],

$$\mathbf{x}^\infty = \mathbf{x}^i + \mathbf{C}(\mathbf{x}^{i+1} - \mathbf{x}^i) \quad (4.2)$$

where,

$$\mathbf{C} = (\mathbf{I} - \mathbf{\Phi})^{-1} \quad (4.3)$$

and

$$\mathbf{\Phi} = \frac{\partial \mathbf{x}(t+T)}{\partial \mathbf{x}(t)} \quad (4.4)$$

- \mathbf{x}^∞ state variables at the limit cycle;
- \mathbf{x}^i state variables at the beginning of the base cycle;
- \mathbf{x}^{i+1} state variables at the end of the base cycle;
- $\mathbf{\Phi}$ discrete transition matrix.
- \mathbf{I} identity matrix

\mathbf{x}^{i+1} can be obtained through integration from \mathbf{x}^i over one period. The proposed process for calculating $\mathbf{\Phi}$ will be detailed in the next section. Once \mathbf{x}^∞ is computed using (4.2), \mathbf{x}^i is equated to \mathbf{x}^∞ and the iteration (4.2) is repeated until consecutive state vectors meet a convergence criterion error.

An important characteristic of $\mathbf{\Phi}$ relies on the fact that the eigenvalues are actually the Floquet multipliers related to the limit cycle, therefore, it is possible to know the stability of the periodic steady-state solution.

This thesis proposes two methodologies for the fast periodic steady state solution of nonlinear electric networks, e.g. a Discrete Exponential Matrix (DEE) and an Enhanced Numerical Differentiation (END), respectively, significantly more efficient than the methods described in [Aprille Jr. and Trick 1972], [Colon and Trick 1973], [Semlyen and Medina 1995], and [Li and Tymerski 2000]. The proposed methodologies are able to compute the limit cycle of nonautonomous nonlinear switched and continuous system. Besides, as this method is based on the shooting method, the stability of the limit cycle can be assessed.

4.3 Discrete Exponential Expansion Method

4.3.1 Recursive Formulation

The dynamics of (4.1) in the neighborhood of the limit cycle can be approximated as,

$$\Delta \dot{\mathbf{x}}(t) = \mathbf{J}(t) \Delta \mathbf{x} \quad (4.5)$$

where $\mathbf{J}(t)$ is the Jacobian of $\mathbf{f}(t, \mathbf{x})$, and is defined as,

$$\mathbf{J}(t) = \mathbf{f}_x(t, \mathbf{x}) \quad (4.6)$$

The solution of (4.5) expressed in discrete times, multiples of T is,

$$\Delta \mathbf{x}_{k+1} = \Phi_k \Delta \mathbf{x}_k \quad (4.7)$$

where,

$$\Delta \mathbf{x}_k = \Delta \mathbf{x}(kT) \quad (4.8)$$

If \mathbf{f} is one-dimensional, then

$$\Phi_k = \exp \int_{kT}^{(k+1)T} \mathbf{J}(t) dt \quad (4.9)$$

Φ_k is the discrete transition matrix of (4.5). For our purpose, it is possible to assume that in the neighborhood of the limit cycle the following approximation of Φ_k applies,

$$\Phi_k \approx \Phi_{k+1} \approx \Phi_{k+2} \approx \Phi_{k+3} \dots \approx \Phi_{k+m} \approx \Phi \quad (4.10)$$

For the multivariable case, (4.9) applies only if the Jacobian matrix $\mathbf{J}(t)$ is constant. However, for practical purposes it can be assumed that if $\mathbf{J}(t)$ exists, then it is possible to take $\mathbf{J}(t)$ constant for small time intervals. Therefore, the solution of (4.5) for the multivariable case, where $\mathbf{J}(t)$ is time-varying can be approximated as [D'Angelo 1970],

$$\Delta \mathbf{x}_{k+1} \approx e^{\mathbf{J}_N \Delta t_N} e^{\mathbf{J}_{N-1} \Delta t_{N-1}} \dots e^{\mathbf{J}_2 \Delta t_2} e^{\mathbf{J}_1 \Delta t_1} \Delta \mathbf{x}_k \quad (4.11)$$

where Δt_i is defined as $t_i - t_{i-1}$, N is the number of intervals in one period and \mathbf{J}_i is,

$$\mathbf{J}_i = \mathbf{f}_x \left((t_i + t_{i-1}) / 2, (\mathbf{x}_i + \mathbf{x}_{i-1}) / 2 \right) \quad (4.12)$$

t_i represents the i -th element of the time vector from t to $t+T$, also \mathbf{x}_i is the state vector corresponding to time t_i .

The equation (4.4) can be directly approximated as,

$$\Phi \approx \frac{\Delta \mathbf{x}(t+T)}{\Delta \mathbf{x}(t)} \quad (4.13)$$

Comparing (4.4), (4.11) and (4.13) it is clear that Φ has the form,

$$\Phi \approx \prod_{i=1}^N e^{\mathbf{J}_i \Delta t_i} \quad (4.14)$$

The expression (4.14) represents the approximated transition matrix Φ based on a discrete exponential expansion [D'Angelo 1970]. It will be applied to obtain the periodic steady state solution of nonlinear systems through a Newton method based on the Poincaré map and extrapolation to the limit cycle procedure. Besides, it will be shown that this approach is significantly more efficient than the methods proposed in [Aprille Jr. and Trick 1972], [Colon and Trick 1973], [Semlyen and Medina 1995], and [Li and Tymerski 2000]. In addition, this formulation is not tied to the numerical integration method used, as is the case of [Aprille Jr. and Trick 1972] tied to the trapezoidal rule and the backward Euler method, instead, (4.14) allows any type of integration method to be used for the determination of Φ . It can be noticed that if $\mathbf{J}(t)$ is piecewise time-invariant, then the exact discrete transition matrix of (4.4) can be computed using (4.14) [D'Angelo 1970]. Equation (4.14) implies that the nonlinear system represented by (4.1) is approximated by successive linear systems for each integration step. In [Armanazi 1973] the computation of Φ is achieved through matrix exponential products, restricted to commuting linear systems. In this contribution, it is demonstrated that Φ can be approximated by matrix exponential products, even for nonlinear-switched systems.

As far as we know, the DEE method detailed in this contribution has not been proposed before to compute the accelerated time domain steady-state solution of nonlinear-switched circuits nor nonlinear power systems.

The Jacobian can be calculated using a numerical, symbolic or automatic differentiation process [Nocedal 1999]. In this investigation, the Jacobian is calculated using the forward-difference approximation [Nocedal 1999]. Considerable savings can be obtained if one notes that for each integration step, the Jacobian \mathbf{J}_i is nearly identical, and thus only the nonlinear and time-varying elements of the \mathbf{J}_i are computed at each integration step.

It is important to notice that Δt_i can be equal to the integration step used during the solution of the system. However, the computation effort for the determination of Φ can be halved if Δt_i is twice the original integration step length.

4.3.2 Identification of Φ

The transition matrix Φ of $n \times n$ dimension, where the number of state variables n is obtained following a step-by-step identification procedure based on a recursive application of (4.14). This is a very efficient process since it is not required the sequential perturbation column-by-column of the state variables and thus, of the numerical integration of n periods of time to fully identify Φ as needed by Newton methods such as the Numerical Differentiation (ND) and Direct Approach (DA), respectively, reported in [Semlyen and Medina 1995]. Instead, each identification of Φ with the DEE method requires of a numerical integration process to be carried-out over a single period (cycle) of time.

4.3.3 Incorporation of Sparsity

Considering the Jacobian numerical structure, it is possible to incorporate sparse matrix techniques to efficiently process the numerical operation involved in the Taylor approximation. The exponential matrices approximated by Taylor series are sparse. Thus,

(4.14) can be efficiently performed using sparse techniques, as it will be demonstrated in Section 4.3.7.2. The sparse solution facility of MATLAB was used for the case studies reported in this thesis.

4.3.4 Variants of the DEE Method

For the practical implementation of the proposed DEE method, two variants named DEE-1 and DEE-2 methods, respectively, have been developed:

- a) DEE-1 method. Here all the elements of the Jacobian are numerically computed at each integration step.
- b) DEE-2 method. In this method, only the nonlinear and time-varying elements of the Jacobian are computed at each integration step.

The efficiency of both methods is further enhanced with the incorporation of the following strategy of solution:

4.3.5 Updating of the Transition Matrix Φ

The computation effort involved for the iterative solution of (4.2) can be considerably reduced if the transition matrix Φ is not updated at each application (iteration) of (4.2) [Colon and Trick 1973]. The proposed procedure to update the transition matrix can be summarized as follows.

Consider $\mathbf{x}^i = \mathbf{x}^\infty$ to be the i -iteration of (4.2) obtained with Φ , then integrate x^i over one period to obtain \mathbf{x}^{i+1} . Compute the new \mathbf{x}^∞ using (4.2) and the last Φ . Finally integrate \mathbf{x}^∞ over one period to obtain $\mathbf{x}^{\infty+1}$.

- 1) If $|\mathbf{x}^\infty - \mathbf{x}^{\infty+1}|/|\mathbf{x}^i - \mathbf{x}^{i+1}| < 0.2$ hold the current Φ
- 2) $|\mathbf{x}^\infty - \mathbf{x}^{\infty+1}|/|\mathbf{x}^i - \mathbf{x}^{i+1}| > 0.2$ recalculate Φ

The 0.2 criterion is an experimentally determined value by the authors. This solution scheme is at the expense of degrading the natural quadratic convergence properties of the Newton method. However, the overall efficiency of the DEE methods is increased as the computational effort is reduced with the proposed updating scheme of Φ .

4.3.6 Computation of the Exponential Matrix

The discrete exponential expansion of (4.11) can be computed in several ways [Moler and Loan 2003]. In practice, it is important to take into account the stability and the efficiency of the method; these features indicate that some of the methods are preferable to others. However, none of them is completely satisfactory, although some are much better than others. In this thesis, the exponential matrix is computed using a scaling and squaring algorithm with a Taylor approximation; however, any other method can be used. For more details about this technique see [Moler and Loan 2003].

4.3.7 Simulation Results

The efficiency and the potential of the proposed discrete exponential expansion method are demonstrated with the periodic steady state solution of the two case studies presented next. The proposed variants of the DEE method, e.g. DEE-1 and DEE-2, respectively, will be compared against the BF [Parker and Chua 1989], ND [Colon and Trick 1973] [Semlyen and Medina 1995], Aprille and Trick method (AT) [Aprille Jr. and Trick 1972], and the Finite Differences (FD) [Parker and Chua 1989] [Nayfeh and Balachandran 1995] methods. The FD method has been programmed using the sparse matrix techniques of MATLAB. The numerical integration process based on the fourth-order Runge-Kutta (RK4) method has been used for the two case studies; however, any other numerical integration method can be used. The process to compute the transition matrix using the algorithm proposed by Aprille and Trick [Aprille Jr. and Trick 1972] with the RK4. The BF, ND, AT, FD, DEE-1 and DEE-2 methods were developed in the MATLAB language. The process to compute the transition matrix using the algorithm proposed by Aprille and Trick based on the RK4 method is detailed in Appendix B. A 2.99 GHz, 0.99 GB, Pentium 4 HT, PC computer was used.

4.3.7.1 Six-Pulse Rectifier

The first case to be analyzed is the six-pulse rectifier of Figure 4.1. The diodes are modeled as ideal switches. Zero initial conditions are used. In order to incorporate nonlinearities in the circuit, the rectifier is connected to the voltage source through a three-phase Δ - Δ transformer, including magnetic saturation effects. The saturation characteristic curve is modeled with the polynomial approximation [Lin, et al. 1989]. The system parameters are given in Table 4.1. The behavior of the system is represented by a set of 9 differential equations. This case study is particularly interesting, since it contains nonlinear variables and noncontinuous states.

TABLE 4.1 SIX-PULSE RECTIFIER PARAMETERS
Voltage Source: 300 V (L-L rms), and phase angle of phase A is 0° .
The load resistor: $R=32 \Omega$.
Transformer parameters: $r_1=0.5 \Omega$, $r_1=0.02 H$, $r_2=0.5 \Omega$, $r_2=0.02 H$; $R_m=5 K\Omega$. $i_m=1.44\phi+4.69\phi^5$ Amp.

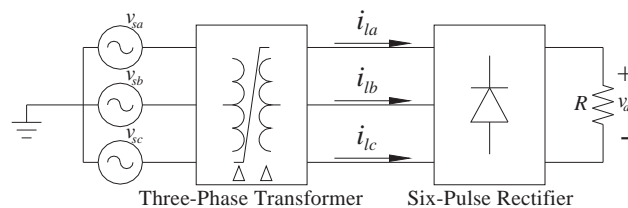


Figure 4.1 Schematic representation of the test system with the six-pulse rectifier

Table 4.2 shows the comparative solution process, in terms of absolute mismatches errors obtained with the ND, FD, DEE-1 and DEE-2 methods. For the six-pulse rectifier case, the AT method does not converge. The DEE-1 and DEE-2 method have the same

convergence error characteristic. Thus, the fourth column of Table 4.2 shows the convergence error for both DEE-1 and DEE-2, respectively

TABLE 4.2 MISMATCHES DURING CONVERGENCE OF THE ND,FD AND DEE METHODS

Iteration	ND	FD	DEE
1	7.44×10^{-2}	7.44×10^{-2}	7.44×10^{-2}
2	4.16×10^{-2}	4.16×10^{-2}	4.16×10^{-2}
3	1.61×10^{-4}	1.61×10^{-4}	1.61×10^{-4}
4	5.58×10^{-9}	5.58×10^{-9}	5.72×10^{-9}

For this particular case, the ND, FD, DEE-1 and DEE-2 methods needed 4 iterations to reach the limit cycle. The steady state solution obtained with the DEE-2 technique is 44.9, 5.5, 6.6, and 1.6 times faster than the BF, ND, FD and DEE-1 methods, respectively. The BF method requires 338 full cycles to reach the steady-state, while the ND needs 54.

The approximation process followed to obtain Φ with (4.14) results on a slightly affected rate of convergence for the DEE method, which can be observed from the fourth iteration; the convergence error is larger than the obtained with the ND and FD method. However, the DEE method is notoriously faster than the ND and FD methods.

The waveforms for the dc voltage across the load resistor v_{dc} and the ac current i_{lc} obtained with SIMULINK solution based on the brute force approach [TEQSIM International Inc 2001], and with the proposed DEE method are shown in Figure 4.2. The high correlation between the solutions obtained with SIMULINK and the DEE method is further illustrated in Figure 4.3, which shows the harmonic spectrum for v_{dc} and i_{lc} .

The reason for the very small discrepancy between the two sets of results is due to the fact that the saturation model in SIMULINK is simulated using piecewise linear relationships between the flux and the magnetization current. Besides, the diode model in SIMULINK includes a snubber resistance and a snubber capacitance.

This case study shows the practical application of the DEE method for nonlinear-switched circuits.

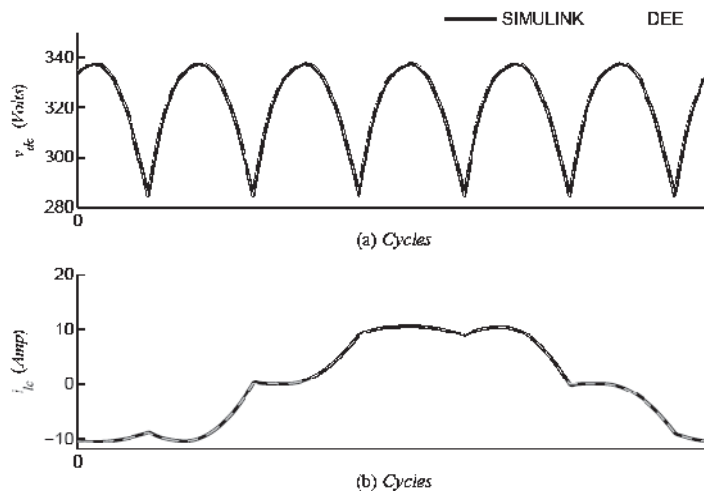


Figure 4.2 Selected waveforms. (a) dc voltage v_{dc} (b) ac current i_{lc} .

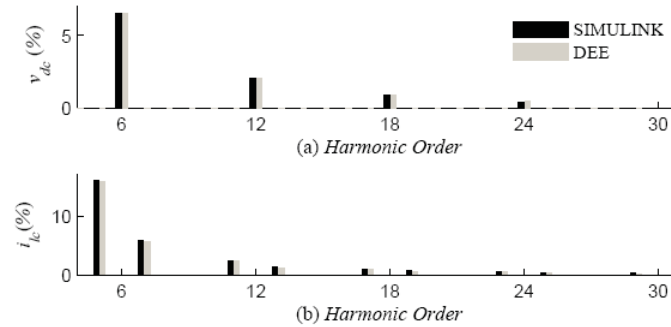


Figure 4.3 Harmonic spectrum for (a) dc voltage v_{dc} , and (b) ac current i_{dc} .

4.3.7.2 Twelve-Node Three-Phase Test System

The 12 node three phase system of Figure 4.4 contains 2 two-winding transformers, with a magnetizing branch each, 14 transmission lines and 10 loads, two are arc furnaces [Acha, et al. 1990] and the rest are represented with RL branches. Three-phase transformers are assumed with the magnetic saturation included, the transmission lines are represented by a π nominal model. The system parameters are given in Table 4.3. The complete power network is represented by a 141 differential-algebraic equation set.

TABLE 4.3 TWELVE-NODE PARAMETERS

Voltage source (v_{G1}): 300 V (L-L rms), and phase angle of phase A is 0° .
Voltage Source (v_{G2}): 300 V (L-L rms), and phase angle of phase A is 20° .
Source voltage impedance ($R_{G1}+j\omega L_{G1}$): $0.1+j\omega 0.001\Omega$. $R_{G1}=R_{G2}$ and $L_{G1}=L_{G2}$.
RL Loads ($R_l+j\omega L_l$): $10+j\omega 0.2\Omega$.
Transmission line parameters: $R=0.1\Omega$, $L=0.03H$, and $C=1\mu F$.
Electric arc furnace parameter: $R_h=1\Omega$, $L_h=5mH$, $K_1=15$, $K_2=0.05$, $K_3=120$, $m=0$, and $n=2$.
Transformer parameter: $r_p=0.05\Omega$, $l_p=5mH$, $r_s=0.05\Omega$, $l_s=5mH$, and $i_m=1.44\phi+4.69\phi^5$ Amp.

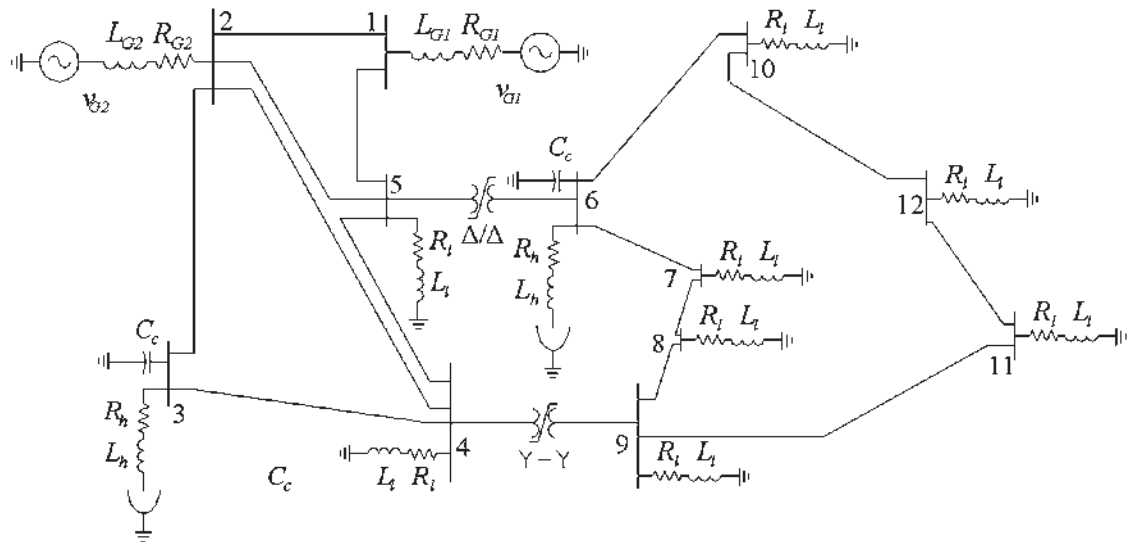


Figure 4.4 Twelve-node three phase test system

Table 4.4 shows the comparative solution process, obtained with the ND, AT, FD, DEE-1 and DEE-2 methods. For this particular case, the ND, AT, FD, DEE-1 and DEE-2 methods needed 5 iterations to reach the limit cycle; the BF method required 2105 cycles, and the ND needs 725.

TABLE 4.4 MISMATCHES DURING CONVERGENCE OF THE ND, AT, FD AND DEE METHODS

Iteration	ND	AT	FD	DEE
1	1.56×10^{-2}	1.56×10^{-2}	1.57×10^{-2}	1.57×10^{-2}
2	1.15×10^{-3}	1.15×10^{-3}	1.15×10^{-3}	1.15×10^{-3}
3	1.76×10^{-4}	1.76×10^{-4}	1.76×10^{-4}	1.76×10^{-4}
4	1.27×10^{-6}	1.27×10^{-6}	1.27×10^{-6}	1.27×10^{-6}
5	1.20×10^{-11}	1.05×10^{-11}	1.51×10^{-11}	6.52×10^{-10}

The DEE-2 method meets the convergence criterion 63.05, 21.11, 6.80, 22.83, and 3.92 times faster than the BF, ND, AT, FD and DEE-1 methods, respectively.

The waveforms for the voltage at bus 6 v_{c6a} , for the voltage at bus 9 v_{c9a} , and for the terminal voltage at the electric arc furnace connected at bus 3 v_{h3a} , obtained with SIMULINK and the proposed DEE methods are shown in Figure 4.5(a), Figure 4.5(b), and Figure 4.5(c), respectively.

The excellent agreement achieved between the solutions obtained with SIMULINK and the DEE methods is further illustrated in Figure 4.6, which shows the harmonic spectrum for v_{c6a} , v_{c9a} , and v_{h3a} .

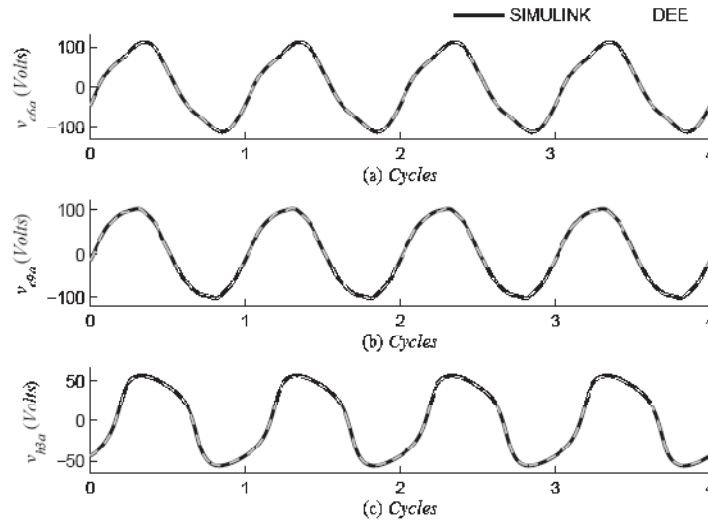


Figure 4.5 Selected waveforms for the twelve-node three phase test system. (a) v_{c6a} , (b) v_{c9a} , and (c) v_{h3a} .

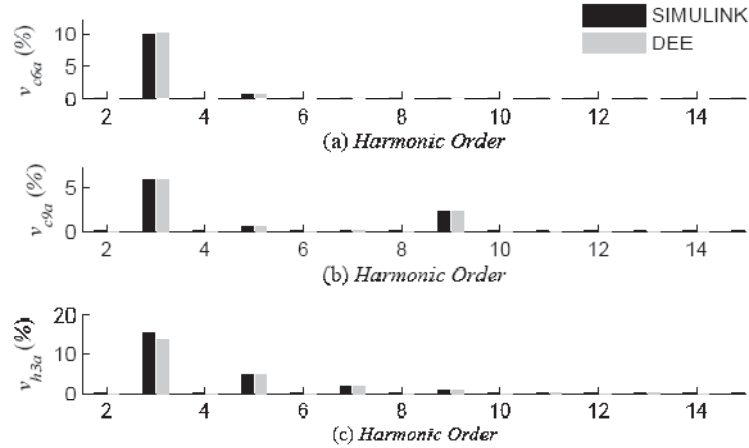


Figure 4.6 Harmonic spectrum for the twelve-node three phase test system. (a) v_{c6a} , (b) v_{c9a} , and (c) v_{h3a} .

(a) *Incorporation of Sparsity Techniques and of the Algorithm to Update the Transition Matrix Φ .*

For the test case of Figure 4.4 only the 2.3% of the elements of the Jacobian matrix are nonzero; this justifies the incorporation of sparse matrix techniques to efficiently carry-out the computation of Φ using (4.14).

Table 4.5 shows the solution process obtained with the DEE method including both the sparse matrix techniques and the algorithm for updating Φ . For this case study, when the algorithm for updating the transition matrix is incorporated in the DEE methods, Φ is computed three times, e.g. in the first, third, and fifth iteration.

TABLE 4.5 MISMATCHES DURING CONVERGENCE OF THE DEE METHOD

Iteration	DEE
1	1.57×10^{-2}
2	5.84×10^{-3}
3	7.94×10^{-4}
4	2.98×10^{-4}
5	4.84×10^{-6}
6	4.62×10^{-8}
7	7.60×10^{-10}

The quadratic convergence characteristic of the DEE method is altered when Φ is not computed at each iteration; however, the computational efficiency is incremented 1.8 times for the DEE-1, and the DEE-2 method, respectively, with the incorporation of the proposed algorithm for the update of Φ and the use of sparsity techniques. The DEE-2 method is now 112.1, 37.5, 12.1, 40.6 and 3.9 times faster than BF, ND, AT, FD and DEE-1 methods, respectively.

4.4 Enhanced Numerical Differentiation Method

The proposed END method is oriented to the accelerated time domain periodic steady state solution of nonlinear power systems; it takes advantage of the half-waveform symmetry of excitation signals, such as voltage sources.

This methodology basically consists on the evaluation of (4.4), by the approximation of $\mathbf{x}(t+T)$ through the extrapolation of $\mathbf{x}(t+T/2)$. With this approximation, the integration of (4.1) for the computation of $\mathbf{x}(t+T)$ is not required to be done over a full period T , as it is usually the case [Colon and Trick 1973], [Semlyen and Medina 1995], [Medina, Ramos-Paz and Fuerte-Esquivel 2003], [Garcia and Medina 2003], [Segundo-Ramírez and Medina 2008] and [Segundo-Ramírez and Medina 2008], but only over a half period, thus increasing the computational efficiency of the ND method in approximately 100%.

Typically, in power electric systems, there are several operating scenarios. The simplest case is when the electric power network is balanced and free of harmonic distortion. Under this condition, the dc signals only have a dc component in their harmonic spectrum, and the ac components only have the fundamental frequency component. The periodic steady state solution of this type of systems can be found by using the phasor concept and a power flow algorithm.

A second case is when the power network is balanced and harmonic distorted. In this operating condition, the dc and ac signals have different harmonic components. The harmonic distortion is produced by the interaction between the power network and nonlinear loads and components, such as saturated transformer inductances, electric arc furnaces, and power electronic devices, among others. Due to the nature of the nonlinear inductances in power transformers, the harmonic components in the ac signals are odd and not multiple of three, except the third harmonic, meanwhile in the dc signal the harmonics components are even and do not contain the fundamental frequency component. For the case of power electronic converters, the harmonic components in their ac side are usually odd and the harmonic components in the dc side are even. The power electronics converter can also produce even harmonic components in their ac side by changing the frequency of the carrier waveform employed in the modulation technique; however, in practice the index modulation is chosen to generate only odd harmonic component in the ac side of the converters and consequently even harmonics components in the dc side [Mohan, et al. 1995].

A more realistic case is when the voltage sources, the load, and the power system are unbalanced and harmonic distorted. However, the characteristic harmonic components in the dc and the ac signal are the same of the second case. Therefore, it can be generalized if the ac signal in the limit cycle satisfies the next equation:

$$x_i(t+T) = -x_i(t+T/2) \quad (4.15)$$

The dc signals cannot satisfy (4.15), since they have in general only even harmonics in practical power systems. Therefore, it is equivalent to say that if a signal satisfies (4.15), then this signal does not have a dc component. On the other hand, the dc signals in the limit cycle satisfy the following equation:

$$x_i(t+T) = x_i(t+T/2) \quad (4.16)$$

Therefore, if a signal satisfies (4.16) in the limit cycle, then it is possible to conclude that this is a dc signal. Furthermore, this dc signal satisfies (4.17).

$$\frac{dx_i(t)}{dt} - \frac{dx_i(t+T/2)}{dt} > 0 \quad (4.17)$$

Summarizing, the proposed END method is based on the following steps:

- 1) To integrate the system (4.1) from t to $t+T/2$.
- 2) To evaluate (4.17); for instance, using finite differences approximations of its derivatives.

This is a simple and fast operation, since it is performed only twice during the solution process. To evaluate (4.17) needs of a very simple operation and it is not a time consuming task. If (4.17) is not satisfied then proceed to integrate the system (4.1) from $t+T/2$ to $t+T$ and use the conventional ND method. On the other hand, if (4.17) is satisfied, identify the dc and ac variables. To do this, it is possible to say that in the neighborhood of the limit cycle, the ac variables satisfy the following equation,

$$x_i(t+T) \approx -x_i(t+T/2) \quad (4.18)$$

and, the dc variables satisfy the following equation,

$$x_i(t+T) \approx x_i(t+T/2) \quad (4.19)$$

With this proposed method we only need to integrate over half period $T/2$, instead of one period T , as in the case of ND method. To apply successfully this method, the solution must be close to the limit cycle, thus a good guess is required.

4.4.1 Simulation Results

4.4.1.1 Three-Phase Electric System Including the Unified Power Flow Controller (UPFC)

In order to proof the proposed method, the test circuit including a Unified Power Flow Controller (UPFC) shown in Figure 4.7 is used. This system contains two three-phase transmission lines between two voltage sources with a fundamental frequency of 60 Hz, and a shift angle of zero. The UPFC is represented with the model proposed in [Segundo-Ramírez and Medina 2009]. It includes the series control proposed in [Fujita, Watanabe and Akagi 2001], and the shunt control proposed in [Mahyavanshi and Radman 2006]. Moreover, the UPFC model has the switching function explicitly represented. The advantage of this model is its applicability to various forms of pulse-width modulation or to other switching strategies. In this contribution, the sinusoidal pulse width modulation (SPWM) technique is used [Mohan, Underland and Robins 1995]. The series and shunt transformers are represented through RL branches.

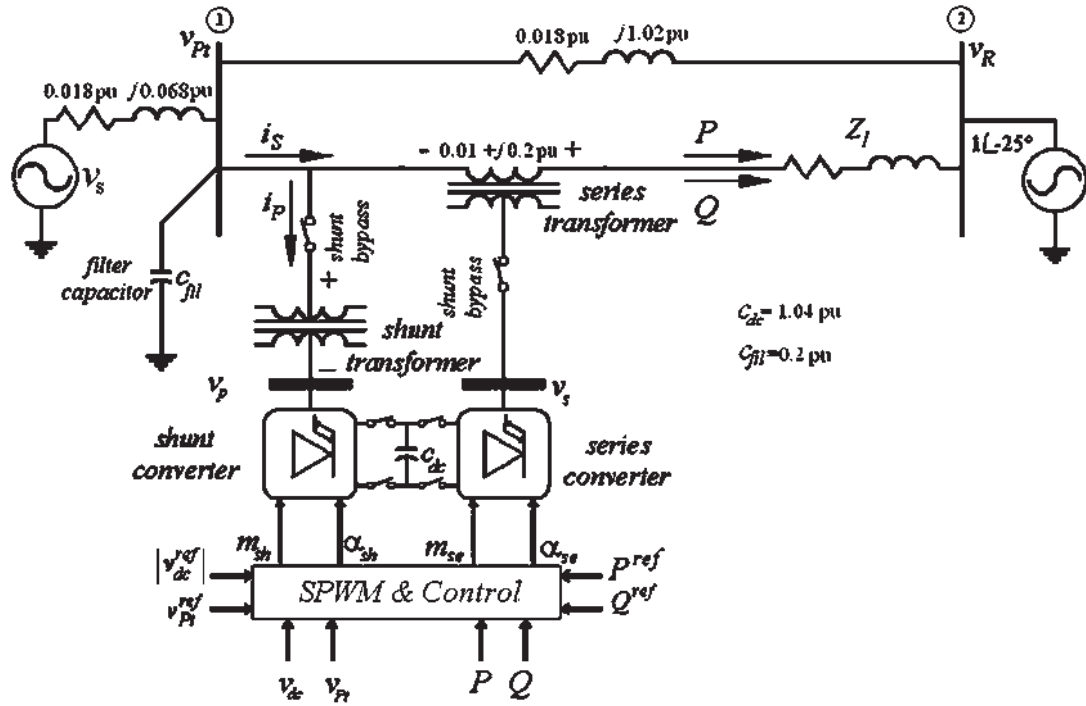


Figure 4.7 Single-phase test system

The reference voltage vector for the series converter is calculated as [Fujita, Watanabe and Akagi 2001],

$$\begin{bmatrix} v_{sd}^{ref} \\ v_{sq}^{ref} \end{bmatrix} = \begin{bmatrix} K_{Sr} & -K_{pSq} - K_{iSq} / s \\ K_{pSp} + K_{iSp} / s & K_{Sr} \end{bmatrix} \begin{bmatrix} i_{sd}^{ref} - i_{sd} \\ i_{sq}^{ref} - i_{dq} \end{bmatrix} \quad (4.20)$$

where i_{sd}^{ref} and i_{sq}^{ref} are the active and reactive reference currents, v_{sd}^{ref} and v_{sq}^{ref} are reference voltages of the series converter, respectively. The active and reactive reference currents are obtained from the active and reactive power flows and by measuring the voltage at the receiving end.

A two-stage control loop scheme is employed for the shunt converter of the UPFC. This scheme has two objectives: to control the voltage across the dc capacitor, and to regulate the ac voltage of the power system bus where the shunt converter is connected. The control scheme is given by

$$\begin{bmatrix} m_{sh} \\ \alpha_{sh} \end{bmatrix} = \begin{bmatrix} K_{pm} + K_{im} / s & 0 \\ 0 & K_{p\alpha} + K_{i\alpha} / s \end{bmatrix} \begin{bmatrix} |v_{Pt}^{ref}| - |v_{Pt}| \\ v_{dc}^{ref} - v_{dc} \end{bmatrix} \quad (4.21)$$

where $|v_{Pt}^{ref}|$ is reference magnitude of the shunt bus, $|v_{Pt}|$ is the instantaneous magnitude of the shunt bus, m_{sh} is the index modulation ratio of the shunt converter and α_{sh} is the phase angle shunt voltage.

The series controller regulates the real ($P_{ref}=0.45$ pu) and reactive ($Q_{ref}=0$ pu) power flows by adjusting the injected series voltage. The shunt converter regulates the dc-side capacitor voltage ($v_{dc}=2$ pu) and the sending end voltage ($|v_{Pt}^{ref}|=0.96$ pu). The modulation index used is $m_f=9$. The limit cycle is reached once a maximum absolute error criterion in the state variables is within 10^{-10} pu. The test system dynamics are represented by a set of 26 ODEs. An integration step of $0.1 \mu\text{s}$ has been used in Simulink, and $33 \mu\text{s}$ and $16.3 \mu\text{s}$, respectively, for the proposed model. The fourth-order Runge-Kutta numeric integration method was used.

The voltage v_s is harmonic distorted with third and fifth components, this voltage is given by

$$\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) + 0.03 \cos(3\omega t) + 0.013 \cos(5\omega t) \\ \cos(\omega t - 2\pi/3) + 0.03 \cos(3\omega t - 2\pi/3) + 0.013 \cos(5\omega t - 2\pi/3) \\ \cos(\omega t + 2\pi/3) + 0.03 \cos(3\omega t + 2\pi/3) + 0.013 \cos(5\omega t + 2\pi/3) \end{bmatrix} \text{ pu} \quad (4.22)$$

In addition, the transmission line connected with the series converter of the UPFC is unbalanced, with $Z_{la} = 0.016 + j1.15$ pu, $Z_{lb} = 0.017 + j1.15$ pu, and $Z_{lc} = 0.018 + j1.15$ pu.

The comparison of CPU times between the proposed method and SIMULINK cannot be done since the proposed method and this simulator are developed in different platforms. However, the comparisons can be carried out using the number of full cycles as a common unit of time instead of seconds. In this case, as the integration step has to be different, the computational efficiency must take into account the ratio of the integration step.

(a) Convergence to the limit cycle

In order to make the damping of the system very low, e.g. with a Floquet multiplier of 0.99, the gains set has been selected as $K_{Sr}=0.566$, $K_{pSq}=1$, $K_{iSq}=0.0029$, $K_{pSp}=1$, $K_{iSp}=0.0029$, $K_{pm}=0.001$, $K_{im}=0.5$, $K_{p\alpha}=0.0005$, $K_{i\alpha}=0.1$.

Table 4.6 shows the results obtained in terms of number of full cycles of time (NFC) required to obtain the periodic steady state solution using two different integration step, e.g. $\Delta t=33 \mu\text{s}$, and $\Delta t=16.3 \mu\text{s}$. In both cases, the performance of the BF, ND and the END is almost the same. The small difference is because the same ODE set is mapped at a different discrete-time system for each integration step. In both cases, the periodic steady state is achieved after 10495 periods using the BF approach based on the RK4 method, after 94 cycles when the ND method is applied, and after 38 cycles when the END method is applied. For $\Delta t=33 \mu\text{s}$, the END method is 2.82, and 356 times faster than the ND method, and the BF method, respectively. For $\Delta t=16.3 \mu\text{s}$, the END method is 2.84, and 361 times faster than the ND method, and the BF method, respectively. In addition, for both cases, the END and the ND methods converge in two and three iterations, respectively. The results in Table 4.6 show that it is more efficient to use the END, since only 38 full cycles are required to locate the limit cycle. In this particular case, the ND method needs one more iteration as compared with the ND method. However, in most cases the END and the ND methods require the same iterations to meet the specified criterion error.

Figure 4.8 shows the computed steady state solution for two different integration steps using the END method, e.g. $\Delta t=33 \mu\text{s}$ and $\Delta t=16.3 \mu\text{s}$, respectively, and an integration step of $\Delta t=0.1 \mu\text{s}$ for Simulink. Figures 4(a) and 4(b) show the dc voltage and the sending end voltage of phase A, respectively. Please notice that these variables achieve their reference values, e.g. 2 pu for the dc voltage capacitor and 0.96 pu for the sending end voltage, respectively. The results show to be in good agreement. It should be remarked that the END method represents a remarkable computational advantage over the BF method, and even over the ND method.

TABLE 4.6 MISMATCHES DURING CONVERGENCE OF THE BF, ND AND END METHODS

NFC	$\Delta t=33 \mu\text{s}$			$\Delta t=16.3 \mu\text{s}$		
	BF	ND	END	BF	ND	END
1	2.00×10^{-1}	2.00×10^{-1}	2.00×10^{-1}	2.00×10^{-1}	2.00×10^{-1}	2.00×10^{-1}
2	6.28×10^{-2}	6.28×10^{-2}	6.28×10^{-2}	6.28×10^{-2}	6.28×10^{-2}	6.28×10^{-2}
:	:	:	:	:	:	:
10	3.78×10^{-3}	3.78×10^{-3}	3.78×10^{-3}	3.78×10^{-3}	3.78×10^{-3}	3.78×10^{-3}
:	:	:	:	:	:	:
24	9.69×10^{-4}	:	5.67×10^{-6}	9.69×10^{-4}	:	5.71×10^{-6}
38	1.32×10^{-3}	1.89×10^{-5}	7.60×10^{-11}	1.32×10^{-3}	1.89×10^{-5}	5.17×10^{-11}
66	9.00×10^{-4}	1.47×10^{-10}		9.04×10^{-4}	2.02×10^{-10}	
94	1.22×10^{-3}	2.25×10^{-15}		1.21×10^{-3}	5.52×10^{-15}	
:	:			:		
10495	9.91×10^{-11}			9.74×10^{-11}		

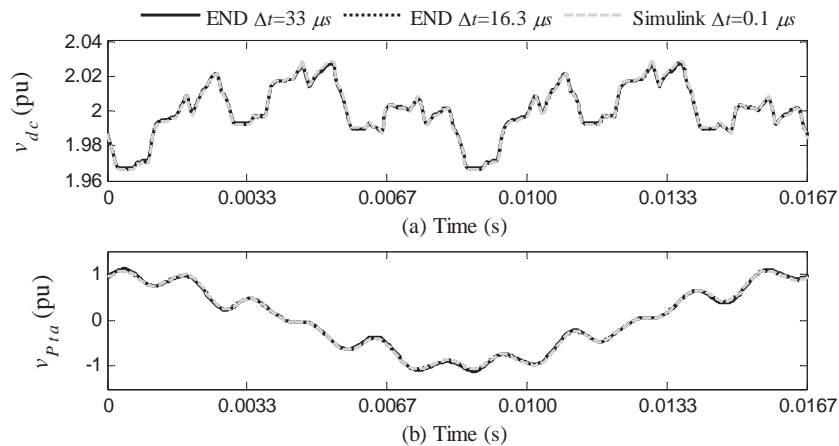


Figure 4.8 Steady-state solution comparison

(b) Harmonic

A close agreement between the Simulink and the END method solutions is obtained, as illustrated in Figure 4.9(a) and Figure 4.9(b), which show the harmonic distortion produced in the dc voltage and the sending end voltage of phase A, respectively. In this Figure, it can be noticed that dc voltage capacitor has only even harmonic components, not only multiple of 6. On the other hand, the terminal voltage and the series current contain only odd harmonic components [Mohan, Underland and Robins 1995]. Please notice that the

spectrum obtained using the END method is in very close agreement for the two different integration steps, and a smaller integration step is needed when the solution is computed with Simulink.

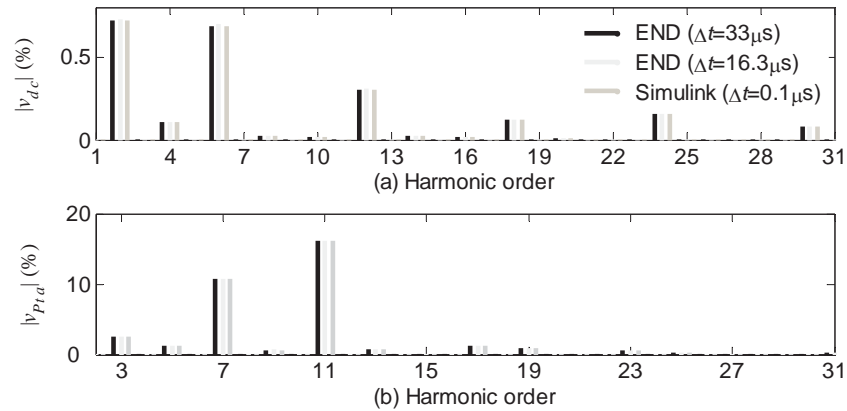


Figure 4.9 Harmonic content comparisons. (a) Harmonic content in the dc voltage. (b) Harmonics in phase A of the terminal voltage. (c) Harmonics in the phase A of the series current

4.5 Conclusion

Newton methods based on a discrete exponential expansion approach and enhanced numerical differentiation process have been proposed for the fast periodic steady state solution in the time domain of nonlinear electric networks using a Poincaré map and an extrapolation to the limit cycle process.

Two variants for the proposed DEE method have been introduced, i.e. DEE-1 and DEE-2. In the DEE-1 method, all the Jacobian elements are obtained numerically, whereas with the DEE-2 method, only the nonlinear and time-varying elements are calculated at each integration step. In all cases, the DEE-2 method is more efficient than the DEE-1 method, since it needs fewer operations to carry-out the computation of Φ .

The proposed DEE methods have been successfully applied for the computation of the periodic steady state solution of a nonautonomous nonlinear-switched system and for larger electric system, e.g. a nonautonomous nonlinear-continuous 12-bus three-phase test system.

The efficiency of the introduced DEE-1 and DEE-2 methods has been further enhanced with the incorporation of sparsity techniques and an algorithm for the updating of Φ during the iterative solution of the DEE method.

It has been observed that for the 12-bus three-phase test system, the incorporation of these strategies of solution resulted in an increase of the DEE-1 and DEE-2 methods computer efficiency. On average, the DEE-2 method was 112, 37.5, 12, 40.6 and 4 times faster than the BF, ND, AT, FD and DEE-1 methods, respectively.

The response given by the proposed methodology has been successfully compared against the periodic steady state solution obtained with the widely accepted digital simulator Power Blockset of SIMULINK for electromagnetic transient studies. In all cases the obtained results have been in close agreement.

On the other hand, a Newton method based on an Enhanced Numerical Differentiation approach has been proposed for the fast periodic steady state solution in the time domain of

nonlinear power networks using a Poincaré map and extrapolation to the limit cycle process.

The proposed END method has been successfully applied for the computation of the periodic steady state solution of nonlinear-switched electric systems. The application END method approximately halved the number of cycles and, therefore, the computation effort needed by the ND method to reach the limit cycle and thus the periodic steady state; even though the ND and END methods have a quadratic rate of convergence.

It has been observed, for the analyzed case studies, that the END method is on average 356 and 2.8 times faster than the BF and ND methods, respectively. The results have been also successfully compared against the response obtained with the power block set of SIMULINK.

5 Stability Analysis Based on Bifurcation Theory of the DSTATCOM and DVR

This Chapter presents the stability analysis for the DSTATCOM operating in voltage control mode, for the DSTATCOM operating in current control mode, and for the DVR. It is shown through the bifurcation theory that the stability boundary of the DSTATCOM on the Thevenin space is limited by the Neimark-Sacker bifurcation. For the case of the stability analysis of the DVR it is shown that fundamental frequency model can give erroneous results if the switching frequency is close to the network frequency. Additionally, it is shown through the bifurcation theory that different stability scenarios can appear if we use detailed models of the power converters including harmonic components.

5.1 Continuation Techniques and Bifurcation Theory

The transient and steady-state response of a system represented by a set of ODEs can be computed by conventional numerical integration methods; this method is known as a Brute Force approach [Parker and Chua 1989]. Therefore the stability of any system can be computed through time domain simulations. However, with bifurcation theory it is possible to predict the system behavior around the operating points without resorting to the numerical integration solution. The results obtained with this analysis can be represented with a bifurcation diagram, which provides qualitative information about the behavior of the steady-state solutions (limit cycles), as physical parameters are varied. At certain points (bifurcation points) infinitesimal changes in system parameters can cause significant qualitative changes in periodic solutions. In general terms, the construction of a bifurcation diagram consists of the following steps [Parker and Chua 1989] [Nayfeh and Balachandran 1995]: a) finding a first periodic steady-state solution; b) based on the first solution, find other equilibrium solutions based on a continuation scheme [Parker and Chua 1989] [Nayfeh and Balachandran 1995], and c) determining the stability of each solution.

Continuation schemes are used to determine how the solutions of a system vary with a given parameter. Implementing a predictor–corrector scheme, a continuation algorithm can trace the path of an already established solution as the parameters are varied. A software package widely used is XPPAUTO [Doedel 1986]; however, this software has not been used in this investigation since it presents convergence problems to trace the bifurcation

diagrams of periodically forced nonlinear - switched systems. In this thesis, the sequential method [Nayfeh and Balachandran 1995] is used as the predictor; in this method, the periodic solution determined in the previous step is used as an initial guess for the periodic solution to be determined in the next step. After the third point, an extrapolation method based on the cubic spline is used as a predictor. The Newton method based on the DEE process [Segundo-Ramírez and Medina 2009] is used as the corrector. This continuation method is schematically explained in Figure 5.1.

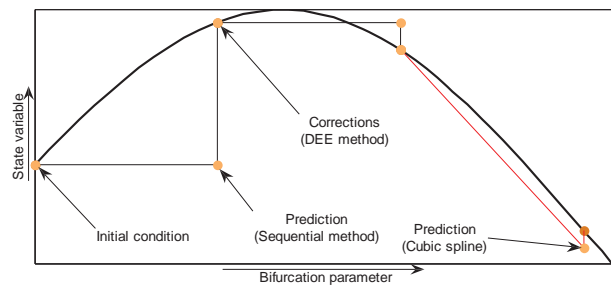


Figure 5.1 Continuation method

The stability of a periodic solution is computed from its Floquet multipliers; they describe the stability near the limit cycle of interest. Floquet theory is based on the observation that a periodic solution can be represented through a fixed point of an associated Poincaré map [Parker and Chua 1989] [Nayfeh and Balachandran 1995]. Consequently, the stability of a periodic solution can be determined by computing the stability of the corresponding fixed point of the Poincaré map. The Floquet multipliers are the eigenvalues of the Jacobian of this Poincaré map. Stable periodic solutions correspond to Floquet multipliers inside the unit circle; on the other hand, unstable periodic solutions have at least one characteristic multiplier outside the unit circle. Therefore, loss of stability is encountered when a multiplier leaves the unit circle; this can occur in three different ways: A fold bifurcation is encountered when a single real Floquet multiplier crosses the unit circle at $+1$. The flip bifurcation or period-doubling bifurcation takes place when a single real Floquet multiplier crosses the unit circle at -1 . At this bifurcation point, the prevailing solution branch becomes unstable and a new branch is born. Solutions on this new branch have twice the period of the previous limit cycle. The generalized Hopf bifurcation or Neimark bifurcation [Parker and Chua 1989] [Nayfeh and Balachandran 1995] is found when two complex conjugated Floquet multipliers leave the unit circle. This bifurcation corresponds to a quasiperiodic solution. This is shown graphically in Figure 5.2.

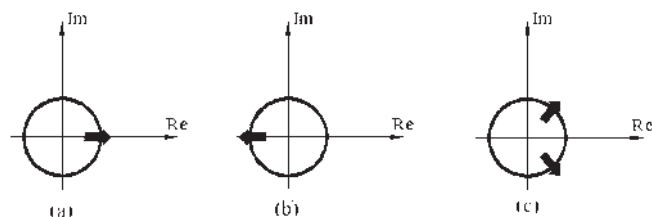


Figure 5.2 Three scenarios for the loss of stability of a solution: (a) Fold bifurcation. (b) Period double bifurcation. (c) Neimark-Sacker bifurcation.

5.2 DSTATCOM Operating in Current Control Mode Stability Analysis Based on Bifurcation Theory

In this Section the bifurcation theory will be applied to the electric system shown in Figure 5.3 to compute the stability regions of the electric system including the DSTATCOM operating in current control mode. The simplified DSTATCOM model presented in Section 3.6.2.2 will be used to carry-out the stability analysis based on bifurcation theory. Additionally, the reference compensation current is computed with (3.32). The stability regions computed through bifurcation analysis are also compared against the time domain simulation using both the detailed and the simplified DSTATCOM models. The stability analysis of the ac electric arc furnace (EAF) based on bifurcation theory and continuation methods has been already presented in [Medina, et al. 2005] [Gomez-Martinez, et al. 2006]; however, in those publications, the ODE set that represents the EAF connected to the power network is not periodically forced.

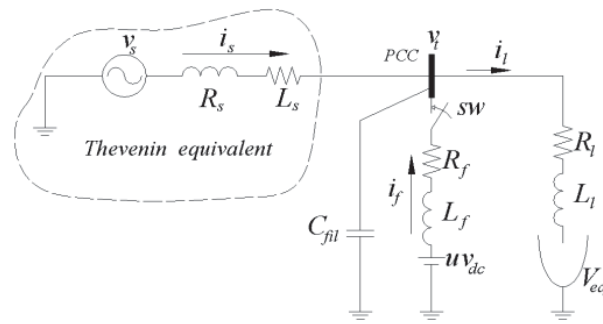


Figure 5.3 Compensation of the EAF when the source is non-stiff and the DSTATCOM contains a passive filter.

5.2.1 Bifurcation Analysis for DSTATCOM in Current Control Mode

5.2.1.1 Stability Regions in the $L_s - R_s$ Plane

The network of Figure 5.3 has been represented through its Thevenin equivalent. The network upstream from the PCC towards the source side may contain different feeders and loads. Thus the radial line and the source shown in Figure 5.3 is a Thevenin representation of the upstream network, where v_s , R_s , and L_s represent the Thevenin equivalent looking towards the left into the network.

Since the Thevenin equivalent can change at any time depending on the load at left side of the PCC, it is desirable to assess a set of v_s , R_s , and L_s , for which the DSTATCOM performance is stable.

For the electric system shown in Figure 5.3, only the Neimark bifurcation was located in the parametrical-space used in this analysis. In analogy with the Hopf bifurcation, a bifurcation is expected at a critical value, as the limit cycle loses its stability, so that an attracting torus is born; this is the secondary Hopf bifurcation or a Neimark bifurcation. Besides, the bifurcated solution can be either stable and supercritical or unstable and subcritical [Nayfeh and Balachandran 1995].

Figure 5.4 shows the bifurcation set on the $R_s - L_s$ plane. This Figure shows the stability regions for different power factor corrections with $|V_s| = 440$ Volts, where $|V_s|$ is the peak value. The solid line represents the Neimark bifurcation set. Inside the contour line the solutions are T -periodic and the gray zones represent the unstable regions. The stable region in the $R_s - L_s$ plane changes according to the power factor at the PCC. For instance, Figure 5.4(d) shows that for a 0.822 lead power factor, an unstable region within the stable region exists. In a practical distribution system, the set (R_s, L_s) is smaller than those stable sets computed through the bifurcation analysis, which means that for all the possible operating points the DSTATCOM operating in current control mode will properly compensate.

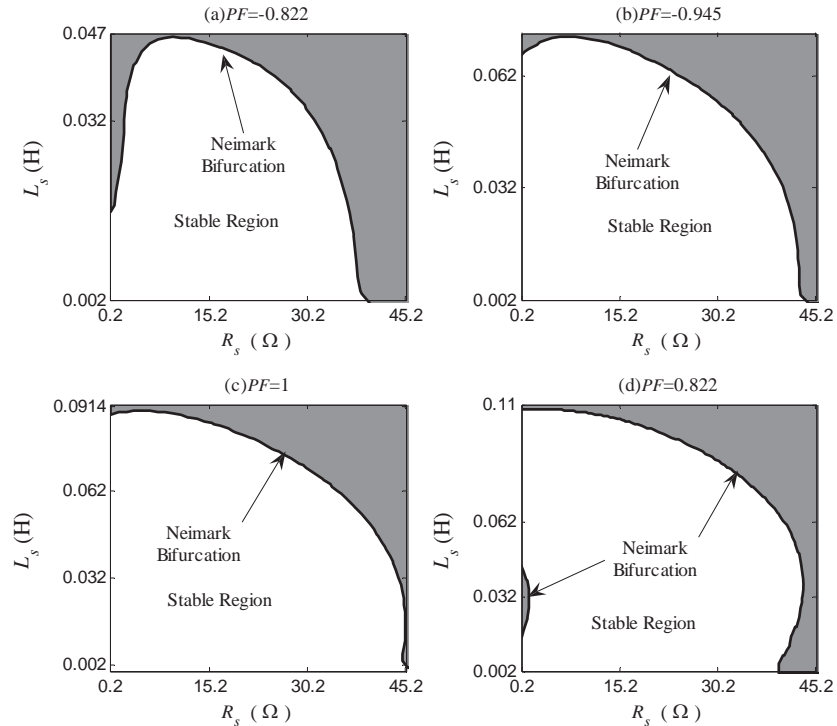


Figure 5.4 Stability regions for the DSTATCOM operating in current control for different power factors at the terminal bus with $|V_s|=440$ Volts

To corroborate the bifurcation diagrams shown in Figure 5.4, time domain simulations were carried-out. Figure 5.5(a) shows phase portrait in the $v_{ta} - i_{lb}$ plane with $PF=1$, $L_s=87.77$ mH, and $R_s=12.1 \Omega$; Figure 5.5(b) shows the phase portrait in $i_{sa} - v_{ta}$ plane with $PF=0.822$, $L_s=30$ mH, and $R_s=1 \Omega$. It is to be noted that only the parameters mentioned above are changed, while the rest of the parameters are those given in Table 3.1. These solutions agree with the bifurcation analyses which predict quasiperiodic solutions. A comparison between the detailed and the simplified models is shown in Figure 5.5; good agreement is achieved between both solutions.

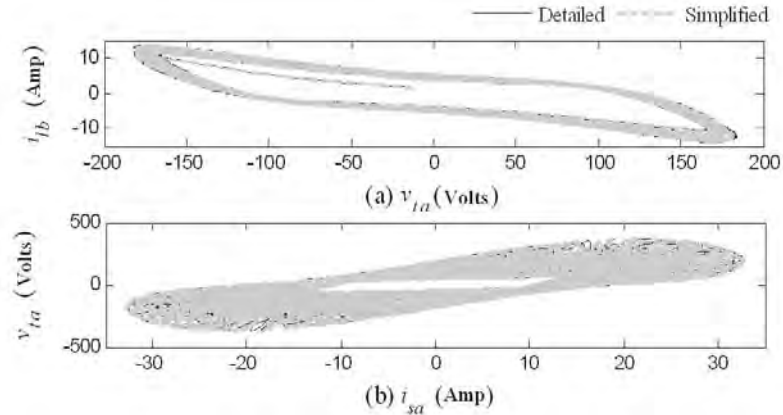


Figure 5.5 Phase portrait for different operating points. (a) Phase portrait in the $v_{ta} - i_{ib}$ plane with $PF=1$, $L_s=87.77$ mH, and $R_s=12.1 \Omega$. (b) Phase portrait in the $i_{sa} - v_{ta}$ plane with $PF=0.822$, $L_s=30$ mH, and $R_s=1 \Omega$

Figure 5.6 shows the simulated waveforms for the compensation current i_{fa} , the dc capacitor voltage v_{dc} , and the terminal voltage v_{ta} , for $PF=1$, $L_s=87.77$ mH, and $R_s=25 \Omega$. For this operating point the dc capacitor voltage suddenly collapses around 0.65 s. This operating point is in the unstable region; however, since it is far from the Neimark bifurcation, the dc capacitor voltage collapses, as shown in Figure 5.6(b). In Figure 5.6 only the solution with the detailed model is presented, since as we mentioned above, the simplified model does not give exact time domain solutions for $v_{dc} \leq 0$. However, it has correctly predicted the loss of stability, as shown in Figure 5.4(c). In addition, the bifurcation diagram (Figure 5.4(c)) predicts the loss of stability due to the emergence of a Neimark bifurcation. Please notice the presence of oscillations in the time domain solution shown in Fig. 5.3. It indicates the existence of a Neimark bifurcation, which agrees with the predicted behavior by the simplified model.

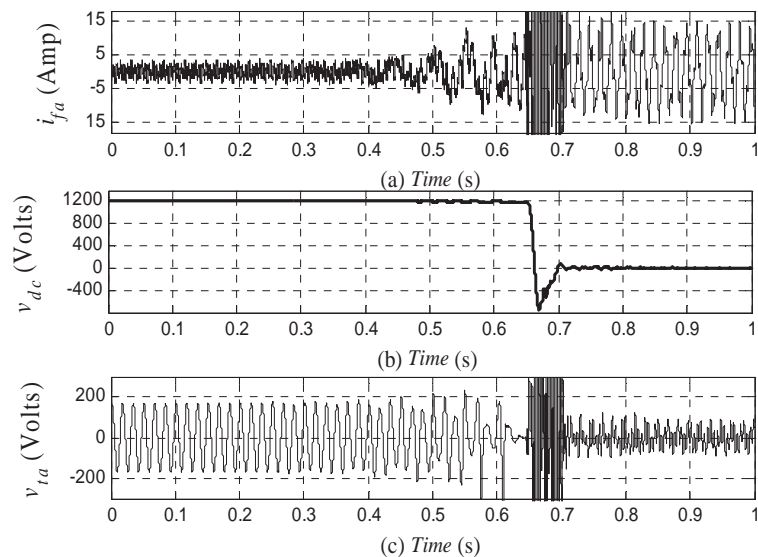


Figure 5.6 Simulated waveforms for $PF=0$, $L_s=87.77$ mH, and $R_s=25 \Omega$. (a) Compensator current i_{fa} . (b) dc capacitor voltage v_{dc} . (c) Terminal voltage v_{ta}

To show the impact of the Thevenin equivalent voltage on the stability regions in the L_s - R_s plane, Figure 5.7 shows the bifurcation set for $|V_s|=440$, 400, and 300 Volts with $PF=1$. Figure 5.7 shows that the stable regions in the $R_s - L_s$ plane decrease as the Thevenin voltage decreases. This is an important observation, since voltage sags can collapse the system if this is operating near a Neimark bifurcation.

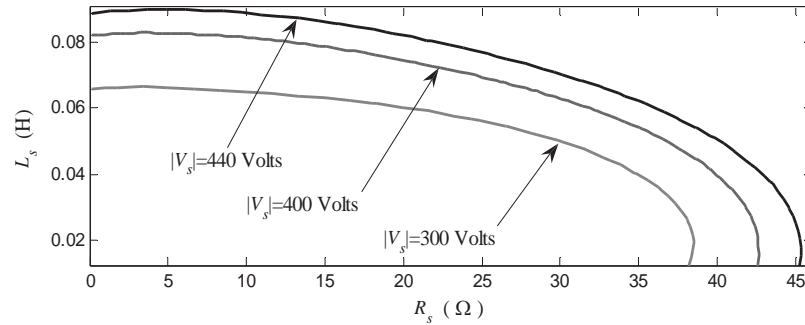


Figure 5.7 Stability regions for the DSTATCOM operating in current control for $|V_s|=440$ Volts, for $|V_s|=400$ Volts, and for $|V_s|=300$ Volts with $PF=1$

5.2.1.2 Stability Regions in the Gains Plane.

In this section, we compute the stability region in the $K_{idc} - K_{pdc}$ space, and in the $K_{i\beta} - K_{p\beta}$ space, as well as the contour lines for different Floquet multipliers.

Figure 5.8(a) shows the stability regions in the $K_{idc} - K_{pdc}$ space, and Figure 5.8(b) shows the stability regions in the $K_{i\beta} - K_{p\beta}$ space. Also, in these figures, contour lines are presented for different Floquet multipliers to show the different speed of response. For example, from the Figure 5.8(a), it is easy to notice that the pair of gains $K_{idc} = 80000$ and $K_{pdc} = 1040$ give the fastest response. The implementation of this set of gains in a physical controller depends on the precision available in the hardware and software employed.

Figure 5.9(a) shows time domain simulations of the convergence error for $K_{pdc} = 1040$ and different K_{idc} . It can be observed that this agrees with the bifurcation diagram of Figure 5.8(a). From Figure 5.8(b), it is easy to notice that in the stable region, there is an important area for which the maximum Floquet multiplier is constant. This means that for this area, the speed of response should almost be the same. To corroborate this observation, the convergence error for $K_{p\beta} = 1.5$ and different $K_{i\beta}$ is shown in Figure 5.9(b). As expected, the convergence error is almost the same in this area.

Figure 5.10 shows the torus solution for compensation current i_f for $K_{p\beta}=0.5$, $K_{i\beta}=300$, $K_{pdc}=1040$, and $K_{idc}=2.5 \times 10^5$. This operating point corresponds to a quasiperiodic solution. Note that the detailed model and the simplified model are in very good agreement, even in the unstable regions.

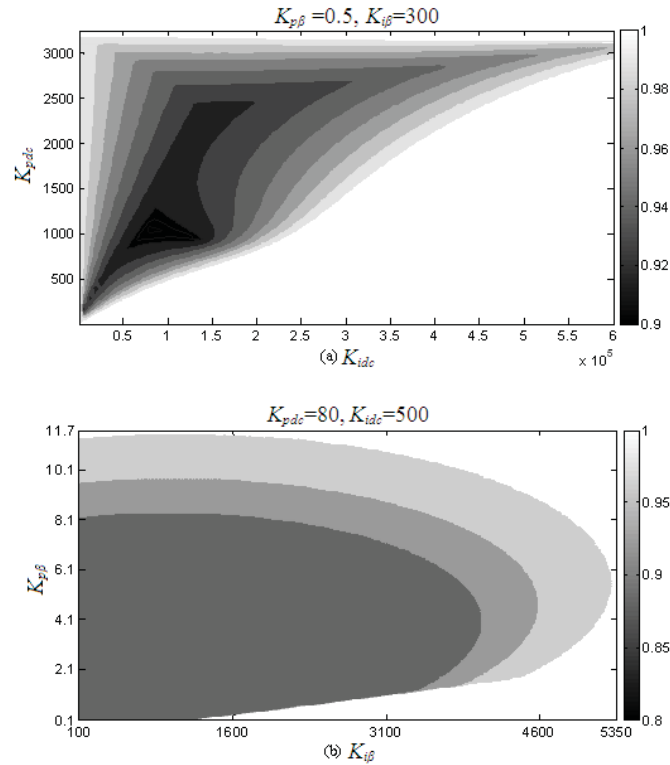


Figure 5.8 Stability regions for the DSTATCOM operating in current control mode in (a) the $K_{idc} - K_{pdc}$ space, and (b) $K_{i\beta} - K_{p\beta}$ space

The correlation between the speed response of the DSTATCOM and its stability is shown in the Figure 5.11. This Figure shows two bifurcation sets in the $R_s - L_s$ plane for two different sets of gains. The first one correspond to the nominal gains given in Table 3.1, and the second one corresponds to the fastest set of gains for the nominal electrical parameters given in Table 3.1. From Figure 5.11 it is possible to observe that the stable region decreases as the speed of response becomes faster. The set of gains can be selected through an assessment of bifurcation diagrams, such as those shown in Figure 5.11.

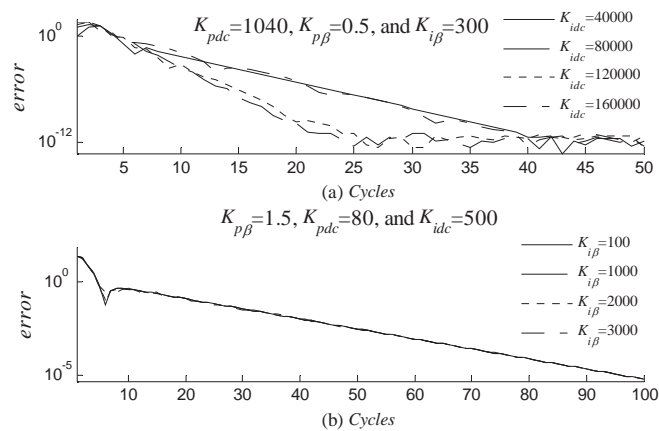


Figure 5.9 Convergence error for different gains in the DSTATCOM controllers. (a) For dc capacitor voltage controller. (b) For power factor controller

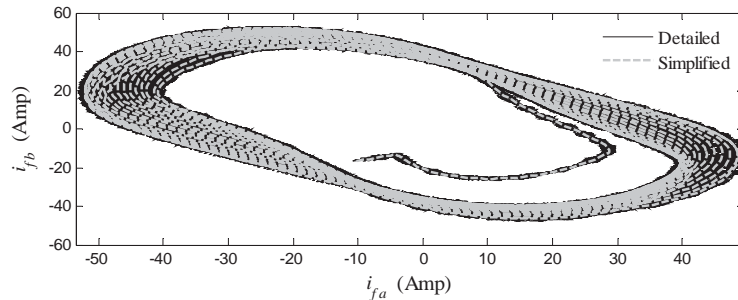


Figure 5.10 Quasiperiodic solution for $K_{p\beta}=0.5$, $K_{i\beta}=300$, $K_{pdc}=1040$, and $K_{idc}=2.5 \times 10^5$. i_{fa} v.s. i_{fb}

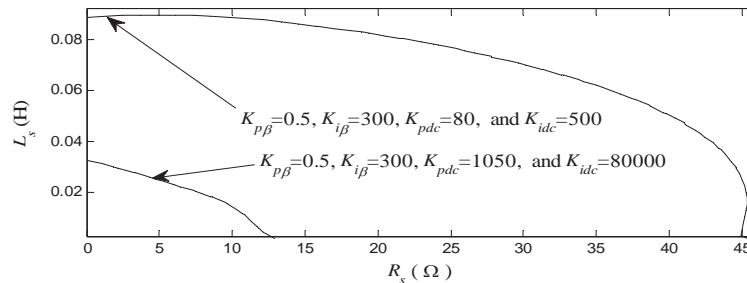


Figure 5.11 Comparison between the stability regions for two different set of gains

5.2.1.3 dc Capacitor Impact on the Stability

The impact of the dc capacitor size in the stability regions in the $R_s - L_s$ plane is qualitatively shown through bifurcation analysis. This analysis shows that the stable region increases as the dc capacitor size increases. However, as the capacitor size becomes larger than a certain value, the stable region remains constant. From this analysis, the size of the dc capacitor can be chosen to suit the load demand. Figure 5.12 shows the stability regions in the $R_s - L_s$ plane for different dc capacitor sizes.

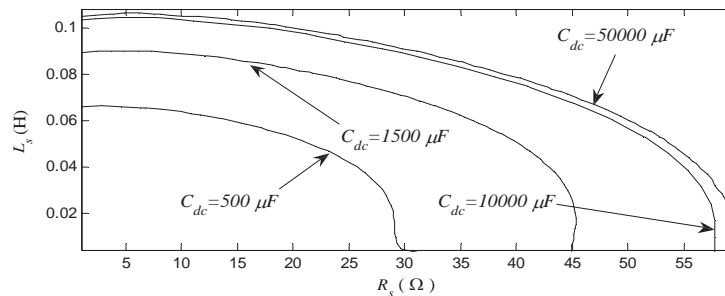


Figure 5.12 Comparison between the stability regions for different dc capacitors

5.2.1.4 ac Capacitor Impact on the Stability

The purpose of the capacitor filter C_{fil} is to provide a path for the switching harmonic current introduced by the DSTATCOM. However, it is shown in [Ghosh and Ledwich 2003], that this passive filter has an important impact on the DSTATCOM performance and on its stability. High capacitances in the capacitor filter provide a low impedance path for the harmonic currents. However, there are three problems related to high capacitances. The first one is the cost, the second one is that the speed of response becomes slower, and the

third one is that the stable region decreases as the capacitance becomes larger. This is shown in Figure 5.13, where the stability region in the $R_s - L_s$ plane has been computed for three different capacitor filters.

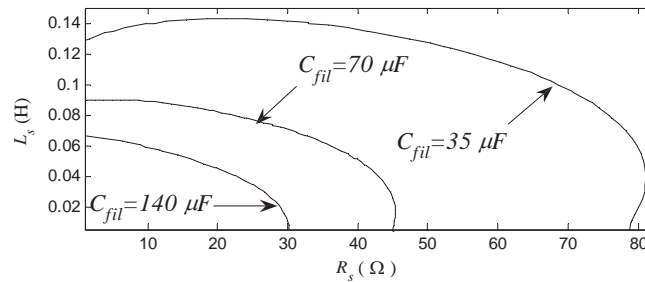


Figure 5.13 Comparison between the stability regions for different ac capacitors

5.2.1.5 Discussion of the Results

With the tracing of bifurcation diagrams, an accurate portrait is drawn for the dynamic system, and the operating zones have been delimited.

Variation in the Thevenin equivalent can cause the limit cycle to loss stability. This is because a Neimark bifurcation appears. The periodic solutions in the unstable region near to the Neimark bifurcation become quasiperiodic and an attracting torus is born. However, for the operating points in the unstable region far from the Neimark bifurcation, the system collapses, as shown in Figure 5.6.

With the tracing of bifurcation diagrams in the gains plane, the operating zones are also delimited and the speed of response of the DSTATCOM known. It is also shown in Figure 5.11 that for slower speed response of the DSTATCOM, the stable region is increased.

The dc capacitor size asymptotically increases the stable region as this becomes larger. Beyond certain value the stable region remains nearly constant.

An interesting result is shown in Figure 5.13. The ac capacitor filter connected at PCC bus to eliminate the high frequency component of the current injected by the DSTATCOM has an adverse effect on the stability. For a small ac capacitor filter the impedance for the harmonic current is high. Therefore, some harmonic currents injected by the DSTATCOM remain in the system. On the other hand, for a larger ac capacitor filter, the impedance to the harmonic currents is low. In consequence, the harmonic current is efficiently drained by the passive filter. Unfortunately, the stable region decreases as the ac capacitor filter becomes larger.

The bifurcation diagrams have been successfully verified through time domain simulations using both the simplified DSTATCOM model and the detailed DSTATCOM model, demonstrating that the stability regions have been correctly computed using the bifurcation theory. However, there are some aspects that must be emphasized to avoid misunderstanding of the results. For instance, for the stable region computed through the bifurcation theory there is a set of initial conditions for which the DSTATCOM properly compensates. This set of initial conditions is not known with the bifurcation analysis. However, for the unstable regions there are not any initial conditions for which the DSTATCOM properly compensates.

For example, Figure 5.12 shows that after certain capacitance of C_{dc} , the stable region remains constant in spite of the size of C_{dc} . However, in this figure it is not possible to notice that the energy in the storage capacitor is higher as the capacitance of C_{dc} becomes larger. Consequently, the DSTATCOM will be able to compensate larger and more serious disturbances in the network because the set of initial conditions for which the DSTATCOM compensation properly increases.

5.3 Bifurcation Analysis for DSTATCOM in Voltage Control Mode

In this section, the bifurcation theory is applied to the electric system shown in Figure 5.3 to assess the stability regions of the electric system including the DSTATCOM operating in voltage control mode. The bifurcations in a power system are basically produced by the nonlinear loads and nonlinear elements. In particular, the DSTATCOM is a nonlinear element due to its controllers and its compensation algorithm.

In the section to follow, bifurcation diagrams in the Thevenin space are computed to show the set of L_s , R_s , and v_s (derived from Thevenin reactance) for which the DSTATCOM contains stable solutions. The stability regions on the gains space are calculated through bifurcation theory, and the set of gains for the fastest speed response of the DSTATCOM is obtained from this analysis. Besides, the gains impact on the stability regions in the Thevenin space is analyzed. Finally, the ac and dc capacitors size impact on the stability in the Thevenin space is analyzed.

The simplified DSTATCOM model presented in Section 3.6.3.1 is used in this analysis; however, the solutions will be compared against the detailed DSTATCOM model to validate the results. The simplified model is used in this analysis rather than the detailed model basically because the detailed model does not allow the correct implementation of the shooting method during the correcting process in the computation of the bifurcation branches through the continuation methods.

5.3.1 Stability Regions in the $R_s - L_s$ Plane

In general, there may be various feeder segments and load buses before the PCC. Therefore, at the best, the source and feeder impedances are the Thevenin equivalent obtained by looking into the network at the PCC. Thus, not only is the feeder impedance unknown a priori, it may suddenly change depending on the loads connected upstream. A non-stiff source supplying a load is shown in Figure 5.3. Here, v_s , R_s , and L_s represent the Thevenin equivalent looking towards the left into the network. The nonlinear load is a three phase EAF [Acha, Semlyen and Rajakovic 1990] looking towards the right into the network. In addition, there is a filter capacitor connected at the PCC bus. Since the Thevenin equivalent can change any time depending on the load at the left side of PCC, it is desirable to assess the set of v_s , R_s , and L_s , for which the DSTATCOM performance is stable.

For the electric system shown in Figure 5.3, only the Neimark bifurcation [Nayfeh and Balachandran 1995] was located in the parametrical space used in this analysis. The Figure 5.14 shows the bifurcation set on the $L_s - R_s$ plane for different Thevenin voltages. The dotted line represents the Neimark bifurcation set. Inside the contour line the solutions are

T -periodic, and the dark zone is the unstable region. The stability region for $|V_m|=350$ Volts, $|V_m|=400$ Volts, and $|V_m|=440$ Volts, are shown in Figure 5.14(a), Figure 5.14(b), and Figure 5.14(c), respectively. In Figure 5.14(d) a comparison is presented between the different stability boundaries; the stability region decreases as the source voltage becomes smaller. Also, Figure 5.14(a) to Figure 5.14(c) can be seen as bifurcation diagrams in the Thevenin space. These stability regions in the Thevenin space can be adjusted through a least-squares exercise to an analytical expression, thus, allowing to have the complete information on the three-dimensional space stability of the Thevenin equivalent, without having to show a bifurcation diagram in the $L_s - R_s$ plane for each Thevenin voltage v_s .

Selected waveforms for $R_s=1 \Omega$, $L_s=2$ mH, and $|V_m|=440$ Volts are shown in Figure 5.15. The voltage across the dc capacitor v_{dc} , the terminal voltage v_{ta} , and the angle δ are presented in Figure 5.15(a), Figure 5.15(b), and Figure 5.15(c), respectively. This behaviour is in agreement with the solution predicted in Figure 5.14(c), since for this set of parameters the bifurcation diagram predicts a quasiperiodic solution. Please notice that for this operating point the dc voltage control given by (3.45) maintains the dc voltage oscillating around its reference. However, the DSTATCOM is not able to efficiently regulate the terminal voltage v_t .

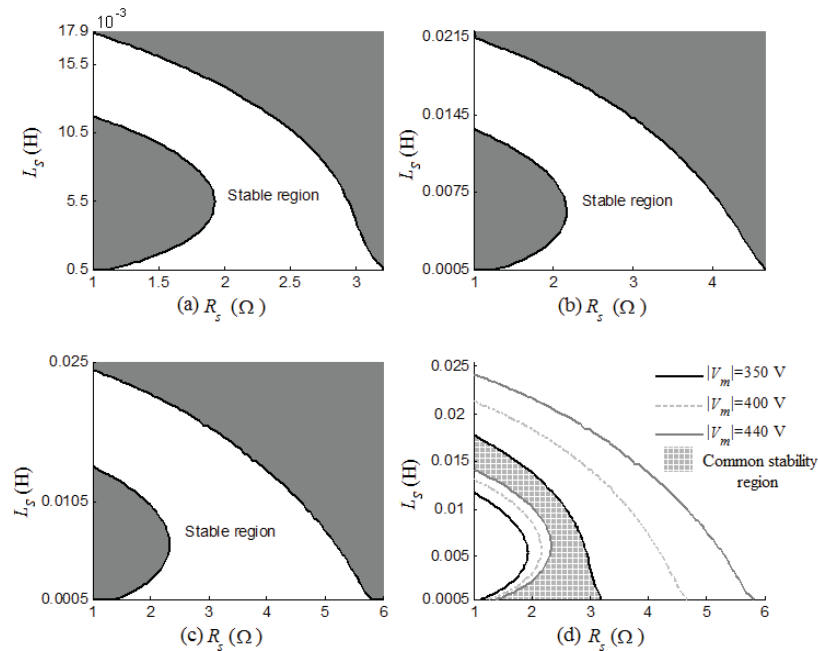


Figure 5.14 Stability regions for the DSTATCOM operating in voltage control in the $L_s - R_s$ plane for different Thevenin equivalent voltages; (a) $|V_m|=350$ Volts, (b) $|V_m|=400$ Volts, and (c) $|V_m|=440$ Volts. (d) Comparison of the stability boundaries.

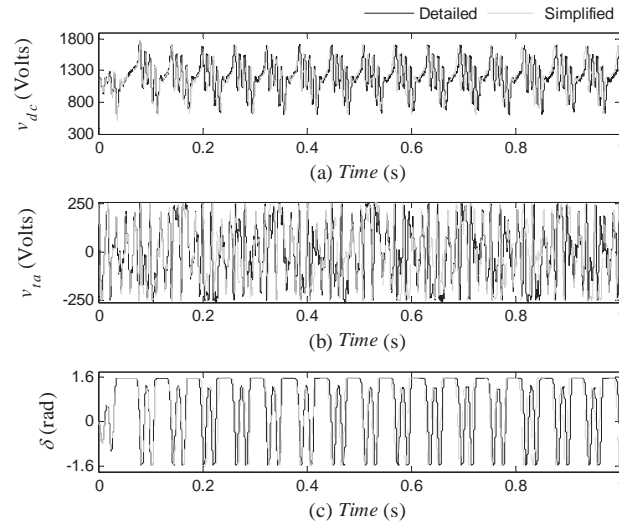


Figure 5.15 Time domain solutions. (a) v_{dc} , (b) v_{ia} , and (c) i_{sa} for $R_s=1 \Omega$, $L_s=0.2$ mH, and $|V_m|=440$ Volts.

Figure 5.14(d) shows that the only region for which the DSTATCOM properly operates in the Thevenin space for $|V_m|$ is from 350 Volts to 440 Volts; between the inner stability boundary of $|V_m|=440$ Volts and the outer stability boundary of $|V_m|=350$ Volts. In this region, the DSTATCOM can compensate any disturbance from the network. To corroborate this observation, various time domain simulations were carried-out for different Thevenin voltages. The $R_s - L_s$ set used for these simulations were $R_s=1 \Omega$, and $L_s=20$ mH. Initially, the system including the passive filter capacitor is in periodic steady-state with the nominal parameters given in Table 3.2; then, the DSTATCOM is connected at $t=0$ s. At $t=0.5$ s the Thevenin voltage magnitude is changed from $|V_m|=440$ Volts to $|V_m|=400$ Volts; for this operating point, the DSTATCOM properly compensates, as we expected from Figure 5.14(d). However, when $|V_m|$ is decreased to $|V_m|=380$ Volts for $t \in [1, 1.7)$ s, the electric system becomes unstable and a quasiperiodic solution appears. At $t=1.7$ s $|V_m|$ is increased to $|V_m|=500$ Volts; for this operating point the DSTATCOM correctly compensates. Now, $|V_m|$ is increased to 850 Volts at $t=2.2$ s; for this operating point a Neimark bifurcation appears. All these changes in the Thevenin voltage are shown in the waveforms of Figure 5.16. The dc capacitor voltage v_{dc} is shown in Figure 5.16(a) and the angle δ in Figure 5.16(b). Please notice that the detailed and the simplified models are used to conduct the time domain simulation and both models are in excellent agreement. These observations agree with the bifurcation diagrams shown in Figure 5.14. To illustrate the quasiperiodic solution at $|V_m|=850$ Volts, the phase portrait in the $v_{dc} - \delta$ plane is shown in Figure 5.17.

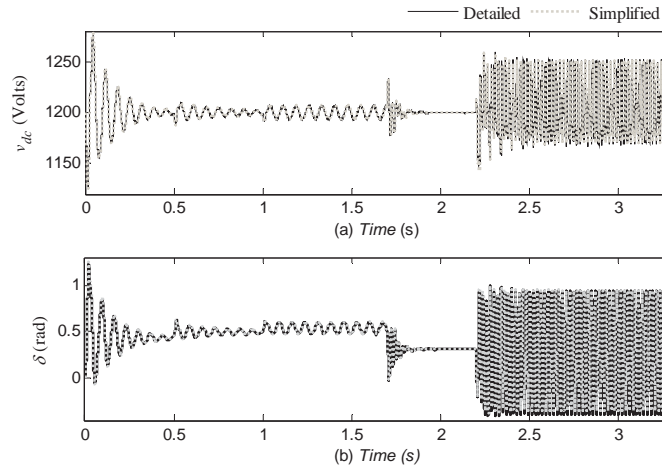


Figure 5.16 Time domain solutions. (a) v_{dc} , and (b) δ

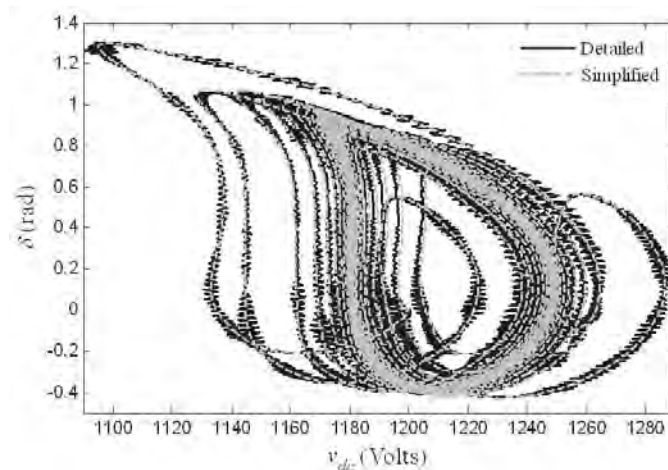


Figure 5.17 Phase portrait in the $v_{dc} - \delta$ plan for $|V_m|=850$ Volts.

5.3.2 Stability Regions in the Gains Plane.

The dynamic behaviour of the DSTATCOM in transient state is strongly related to the gain of the PI controllers; therefore, an important task to do deals with the proper gains assessment. In addition, the set of gains has an important impact on the DSTATCOM steady state performance, since they modify the stability regions.

In this section the stability region in the $K_{idc} - K_{pdc}$ space, and in the $K_{i\delta} - K_{p\delta}$ space are computed, as well as the contour lines for different Floquet multipliers, with the purpose of assessing the set of gains for which the fastest speed of response is obtained.

Figure 5.18(b) in the $K_{idc} - K_{pdc}$ space. Also, in these figures, contour lines are presented for different Floquet multipliers to show the different speed of response. Figure 5.19(a) shows the convergence error for different pairs of gains $K_{i\delta} - K_{p\delta}$. In Figure 5.19(a), the convergence error for $K_{p\delta}=30 \times 10^{-6}$, and different $K_{i\delta}$ are shown. From this figure, we can see that the fastest response is around $K_{i\delta}=10.5 \times 10^{-3}$ and $K_{p\delta}=30 \times 10^{-6}$. Figure 5.19(b) shows the convergence error for $K_{pdc}=74$, and different K_{idc} . From this figure, it is easy to see that

the fastest response is around $K_{pdc}=74$ and $K_{idc}=1320$. These results are in agreement with the bifurcation analysis illustrated in Figure 5.18(a) and Figure 5.18(b), respectively.

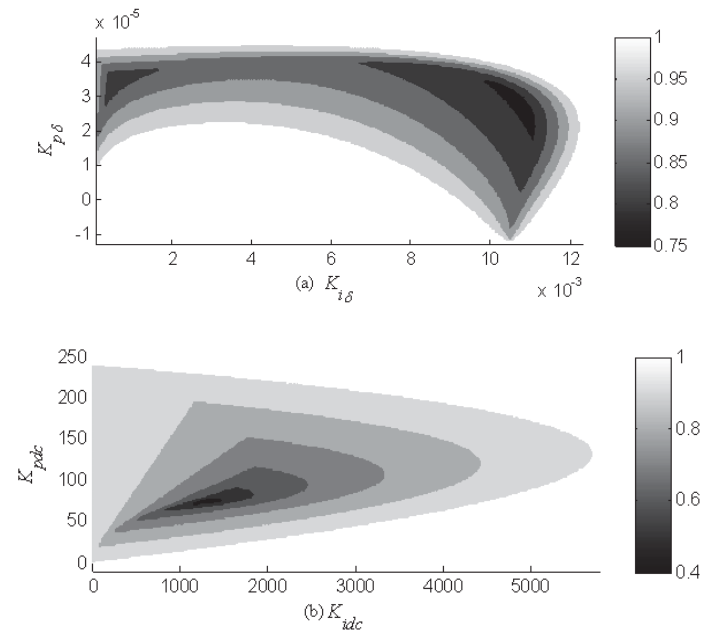


Figure 5.18 Stability regions for the DSTATCOM operating in voltage control mode. (a) $K_{i\delta}$ - $K_{p\delta}$ space. (b) K_{idc} - K_{pdc} space.

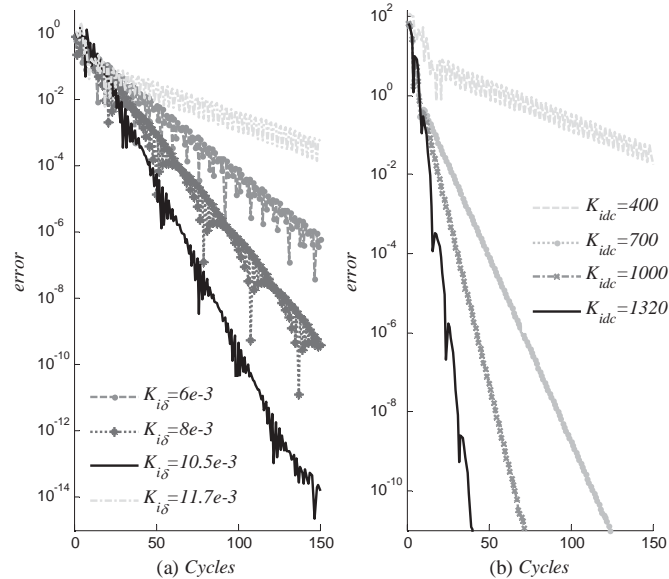


Figure 5.19 Convergence error for different gains of the DSTATCOM controllers. (a) For δ controller. (b) For the dc capacitor voltage controller.

As mentioned previously, the gains of the PI controller have a direct impact on the stability system. However, it is not known how the size of the stable region in the Thevenin space varies when the gains are varied. To investigate the effect of the gains variation in the stability of the system, a bifurcation analysis is carried-out to assess the stable and unstable

regions for different sets of gains. In particular, the stability region obtained for $K_{idc}=1320$, $K_{pdc}=74$, $K_{i\delta}=8\times 10^{-3}$, and $K_{p\delta}=27\times 10^{-6}$ with $|V_m|=440$ Volts is compared against that shown in Figure 5.14(c). This comparison is shown in Figure 5.20; it can be noticed that the size of the stable regions significantly change as we change the set of gains. Figure 5.20 has been computed using the parameters given in Table 3.2; only the gains are varied.

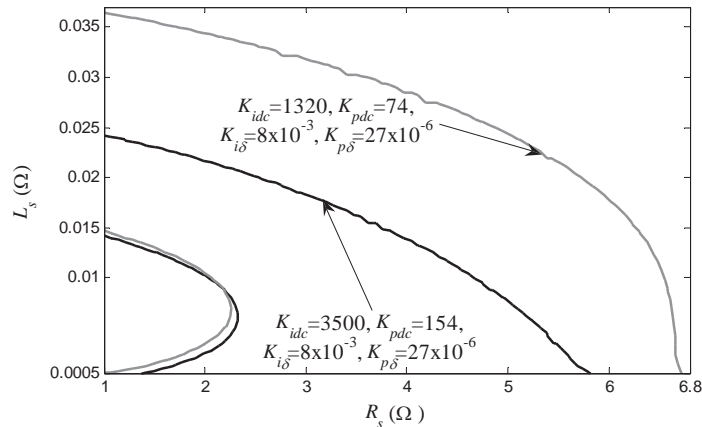


Figure 5.20 Comparison between the stability regions for two sets of gains.

The bifurcation diagrams only show the stability over a parametric region, these do not give us information about the initial condition set for which the trajectories go back to their original steady-state. With the purpose of showing which set of gains shown in Figure 5.20 has a larger attractor, a voltage sag of 41% is produced, and it is defined through simulation that the stability critical recovery time for the set of nominal gains presented in Table 3.2, named set I, is $t_a=0.0212$ s. For the set of gains $K_{idc}=1320$, $K_{pdc}=74$, $K_{i\delta}=8\times 10^{-3}$, and $K_{p\delta}=27\times 10^{-6}$, named set II, $t_b=0.175$ s. The relationship t_b / t_a is 8.25 between the two different sets of gains. For the case of set I, the maximum Floquet multiplier for $|V_m|=440$ Volts and $|V_m|=260$ Volts is 0.88 and 1.43, respectively. For the set II, the maximum Floquet multiplier for $|V_m|=440$ Volts and $|V_m|=260$ Volts is 0.45 and 1.07, respectively. The maximum Floquet multiplier gives information about the limit cycle stability. As previously described, values within the unit circle indicate stable solutions, while external values correspond to unstable solutions. However, it also gives information about the speed of damping attenuation or increase of possible perturbations around the limit cycle. For instance, values close to the unit circle have slow dynamics, whereas farther away values have faster dynamics.

For the case of the response obtained for the set I, it is noticed that the Floquet multiplier in $|V_m|=260$ Volts is larger than the corresponding Floquet multiplier for set II. Therefore, the trajectories during the voltage sag go away more rapidly from the limit cycle corresponding to $|V_m|=440$ Volts for the set I. Thus, in a lesser time the state vector for the set I is outside of the attractor region for the limit cycle corresponding to $|V_m|=440$ Volts.

In conclusion, the set II is better than the set I for three main reasons: First, the response in nominal operation condition is faster, as shown in Figure 5.18. Second, the size of the stable region in the $L_s - R_s$ plane is bigger than the corresponding region for the set I, as

shown by Figure 5.20, and third, its dynamics during the voltage sag is slower, and therefore, it withstands longer duration disturbances.

Figure 5.21(a) and 5.18(b), show the waveforms for δ and the voltage v_{dc} across the dc capacitor, respectively, for the set I of gains. In these figures, the steady state is shown for the first 150 ms; in $t=150$ ms the source voltage drops 41% and it is maintained over 21.2 ms; it then recovers to its pre-fault steady-state, with the DSTATCOM successfully compensating the system. Figure 5.21(c) and 5.18(d) show the waveforms for δ and the voltage v_{dc} across the capacitor for the set II of gains, respectively. The waveforms are obtained as determined for set I, with the only difference being the voltage sag lasting 175 ms.

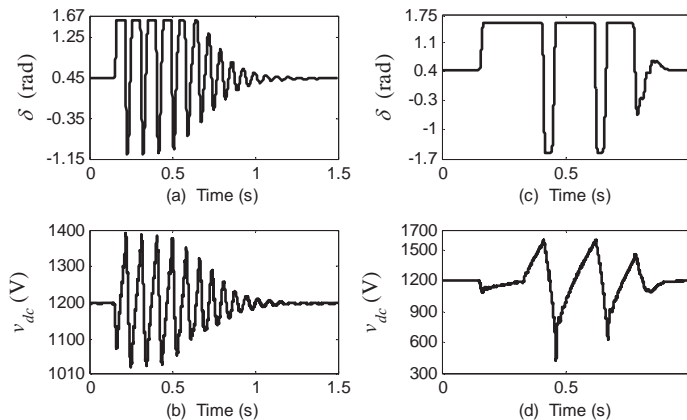


Figure 5.21 Comparison between the transient responses for two set of gains.

5.3.3 dc Capacitor Impact on the Stability Region

The dc capacitor is a very important element in the design of DSTATCOM, as it stores the energy necessary to compensate the load during disturbances. In steady state, the DSTATCOM has to provide the active power fluctuation and the reactive power demanded by the system, in order to maintain the voltage at the PCC bus. Thus, the dc capacitor size is important for the compensator performance; e.g. for large capacitances, the storage energy is high; consequently, the DSTATCOM can bear larger and more severe disturbances. This observation suggests that the stable region increases as the dc capacitor size becomes larger. To corroborate this, a comparison between the stability regions for different dc capacitor sizes is presented in Fig. 15. It can be seen that the stable regions on the $L_s - R_s$ asymptotically increases as the dc capacitor becomes larger. Please notice that even the inner unstable region decreases as the ac capacitor size increases. Figure 5.22 has been computed using the parameters given in Table 3.2. From this analysis, the dc capacitor size can be selected to suit the load demand. Obviously, the selected dc capacitor size also depends on its cost.

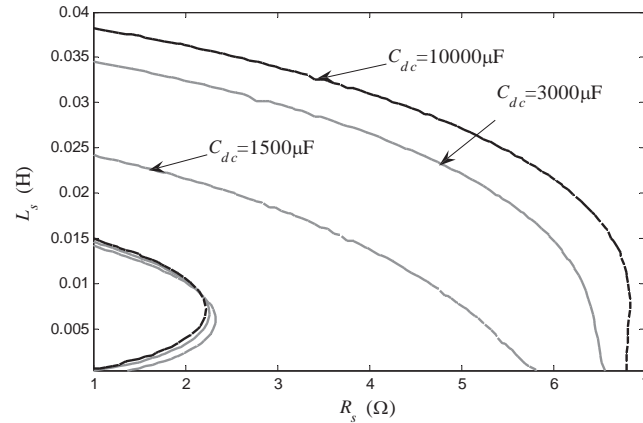


Figure 5.22 Comparison between the stability regions for different dc capacitors.

5.3.4 ac Capacitor Filter Impact on the Stability Region

The main purpose of the ac capacitor filter is to drain the harmonic currents coming from the DSTATCOM converters. A small ac capacitor size presents high impedance to the harmonic currents; in consequence, the harmonic currents are not efficiently drained. For a large ac capacitor size, the harmonic currents are efficiently drained; however, there are some problems with a large ac capacitor filter. For instance, the transients in a capacitor increase as its size increases. To assess the ac capacitor filter impact on the stability, the stable regions in the Thevenin plane have been compared for three different ac capacitors; this comparison can be seen in Figure 5.23. From this figure, it is easy to notice that the ac capacitor has a positive impact on the stability, since the stable region on the $L_s - R_s$ plane increases as the ac capacitor becomes larger. However, it should be noticed that not only the outer boundary increases; the inner boundary becomes larger as well. Basically, the ac capacitor filter size has a positive effect on the stability because the ac capacitor acts as reactive power compensator as well, and this action reduces the reactive power injected by the DSTATCOM to maintain the reference terminal voltage. Figure 5.23 has been computed using the parameters given in Table 3.2.

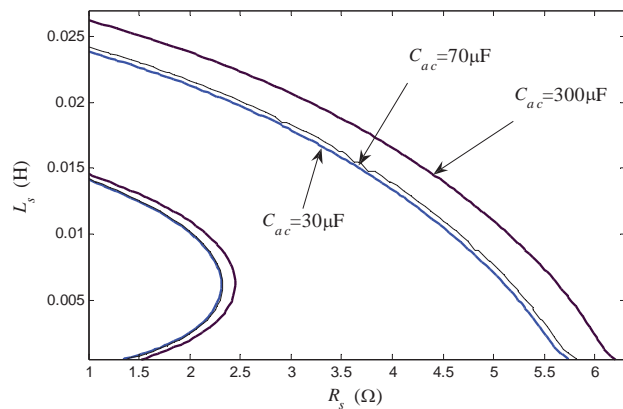


Figure 5.23 Comparison between the stability regions for different ac capacitors.

5.4 DVR Bifurcation Analysis

In this section, the bifurcation theory is applied to the electric system shown in Figure 3.34 to assess its stability regions. For this particular case, the control system used for the DVR is that shown in Figure 3.37; however, another control system can be also used. In the following section, bifurcation diagrams in the Thevenin space are computed to show the set of X_s , R_s , and v_s for which the DVR contains stable solutions. The stability regions on the gains space are calculated through bifurcation theory, and the set of gains for the fastest speed response of the DVR is obtained from this analysis. Besides, the gains impact on the stability in the Thevenin space is analyzed. Finally, the ac and dc capacitors impact on the stability in the Thevenin space is analyzed.

5.4.1 Stability Regions in the $R_s - X_s$ Plane

The network of Figure 3.34 has been represented through its Thevenin equivalent. The network upstream from the PCC towards the source side may contain different feeders and loads. Thus the radial line and the source shown in Figure 3.34 are a Thevenin representation of the upstream network, where v_s , R_s , and X_s represent the Thevenin equivalent looking towards the left into the network.

Since the Thevenin equivalent can change any time depending on the load at the left side of PCC, it is desirable to assess a set of v_s , R_s , and X_s , for which the DVR performance is stable.

5.4.1.1 *Comparison Between the Fundamental Frequency Model and the Detailed Model with Low Frequency Modulation Ratio*

The Figure 5.24 shows the bifurcation set on the $R_s - X_s$ plane computed using the fundamental frequency model of the DVR converter. This figure shows the stability regions for different Thevenin equivalent voltages, e.g., for $|V_s|=0.9$ pu in Fig. 6(a), for $|V_s|=1$ pu in Figure 5.24(b), and for $|V_s|=1.1$ pu in Figure 5.24(c), where $|V_s|$ is the peak value of v_s . The rest of the parameters are those given in the Table 3.3. The solid line represents the Neimark-Sacker [Nayfeh and Balachandran 1995] bifurcation set. This bifurcation corresponds to a quasiperiodic solution. Inside the contour line the solutions are T -periodic. For the electric system shown in Figure 3.34, only the NS bifurcation was located in the parametrical-space using the fundamental frequency model of the DVR converter. Observe that the magnitude of the voltage source has a positive impact on the size of stability regions in the $R_s - X_s$ plane.

To corroborate the bifurcation diagrams shown in Figure 5.24, these are computed again using now the detailed model, which includes the harmonic distortion produced by the converter switching process. The purpose of this simulation experiment is to assess the harmonic interaction between the DVR and the electric system. Figure 5.25 shows the bifurcation diagram computed using the detailed model of the DVR converter. For this analysis, the frequency modulation ratio used is $m_f=9$ (540 Hz), and the highest harmonic order included in this analysis is 113 (6780 Hz). Comparing Figure 5.24 and Figure 5.25, we can observe that the solutions given by the fundamental frequency model and the detailed model are noticeably different. In addition, the detailed model predicts the

supercritical symmetry-breaking bifurcation (Sup. SB), and the NS [Nayfeh and Balachandran 1995]. In the Sup. SB bifurcation, the stable branch of symmetric periodic solutions that exist prior to the bifurcation continues as an unstable branch of symmetric periodic solutions after the bifurcation. In addition, two locally stable asymmetric periodic solutions coexist with unstable symmetry periodic solutions. The maximum and minimum of an asymmetric periodic solution differs.

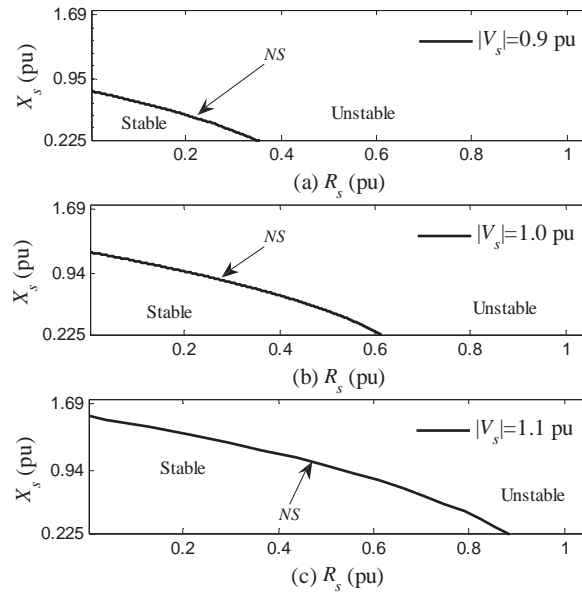


Figure 5.24 Stability regions for the DVR in the $R_s - X_s$ plane for different Thevenin equivalent voltages using the fundamental frequency model.

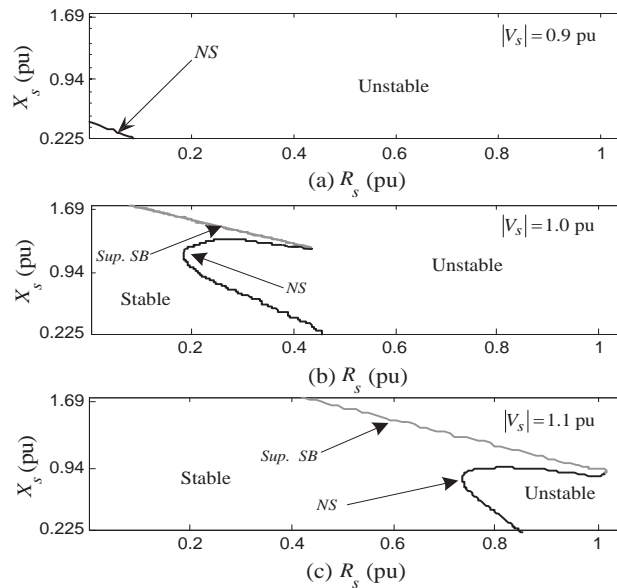


Figure 5.25 Stability regions for the DVR in the $R_s - X_s$ plane for different Thevenin equivalent voltages using the detailed model.

Figure 5.26 shows the bifurcation diagram for $|V_s|=1$ pu, $X_s=1.31$ pu, with R_s taken as the bifurcation parameter. Please notice that close to $R_s=0.405$ pu a supercritical symmetry-breaking bifurcation occurs. Also, a NS bifurcation is born at $R_s=0.325$ pu and disappears at $R_s=0.38$ pu. At $R_s=0.45$ pu, a NS bifurcation is born in the two locally stable asymmetric periodic solutions.

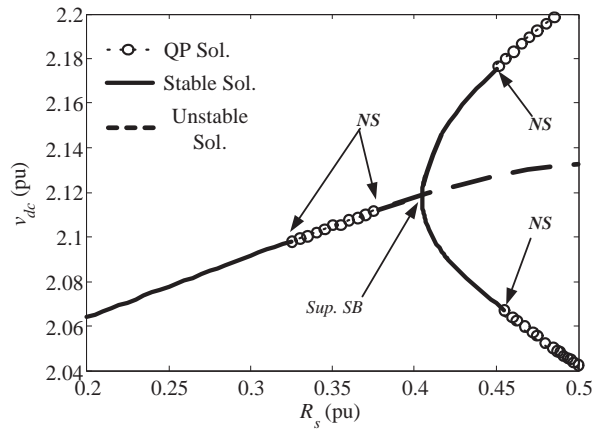


Figure 5.26 Supercritical symmetry-breaking for $|V_s|=1$ pu and $X_s=0.0013$ pu.

Figure 5.27 shows the quasiperiodic(QP) solution in i_{sa} - v_{fa} plane, with $R_s=0.22$ pu, $X_s=1.13$ pu and $|V_s|=1$ pu. This operating point corresponds to a quasiperiodic solution. This solution agrees with the bifurcation analyses which predict quasiperiodic solutions for this operating point.

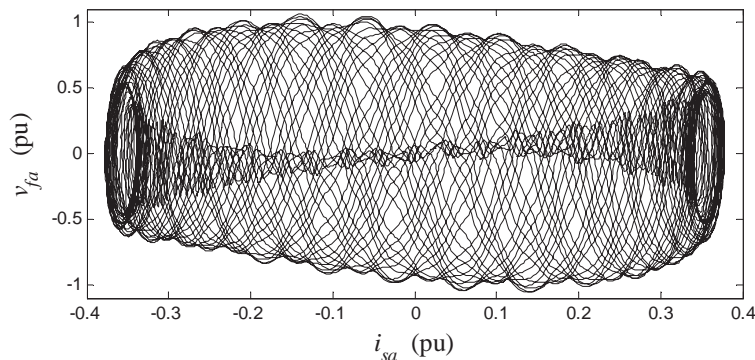


Figure 5.27 Quasiperiodic solution for $|V_s|=1$ pu, $R_s=0.22$ pu, and $X_s=1.13$ pu.

5.4.1.2 Comparison Between the Fundamental Frequency Model and the Detailed Model with Higher Frequency Modulation Ratio

Figure 5.28 illustrates the bifurcation set in the $R_s - X_s$ plane computed using the detailed model of the DVR converter. This figure shows the stability regions for different Thevenin equivalent voltages, e.g. $|V_s|=0.9$ pu in Figure 5.28(a), $|V_s|=1$ pu in Figure 5.28(b), and $|V_s|=1.1$ pu in Figure 5.28(c). For this analysis, the frequency modulation ratio is $m_f = 27$ (1620 Hz), and the highest harmonic order included in the analysis is 113. Please notice that the bifurcation diagrams in Figure 5.28 are identical to those given in Figure 5.24.

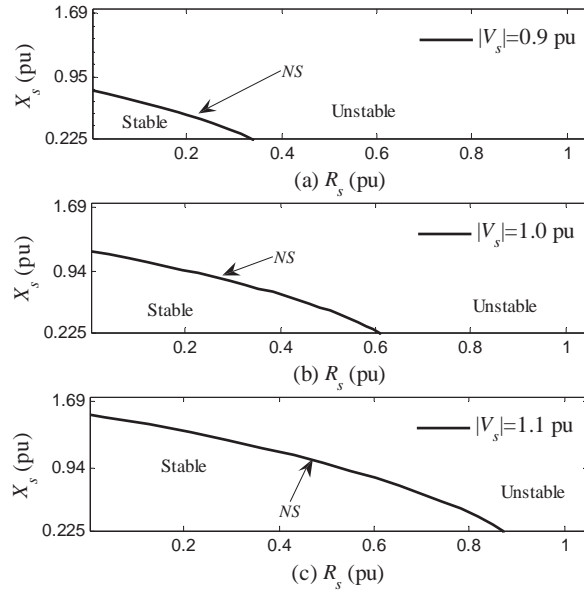


Figure 5.28 Stability regions for the DVR in the $R_s - X_s$ plane for different Thevenin equivalent voltages using the detailed model.

From the conducted experiment, it can be observed that the harmonic distortion has an important effect on the stability of the DVR, thus the harmonic distortion cannot be neglected. Under these conditions, the fundamental frequency model would give erroneous results because the harmonic interaction between the DVR and the electric system is neglected; however, for cases where the switching frequency significantly exceeds the network transient frequencies, the fundamental frequency model would give reliable results.

Hereafter, the frequency modulation ratio used will be $m_f=27$, and the highest harmonic order included in this analysis will be 113.

5.4.2 Stability Regions in the Gains Plane.

The stability region in the gains space is useful for some practical applications: first, it determines the whole set of gains for which the system stability is preserved, and second, because it make easier to know the speed of response directly from the Floquet multipliers.

In this section, the stability region in the $K_{\phi p} - K_{\phi i}$ space, and in the $K_{vp} - K_{vi}$ space is computed, as well as the contour lines for different Floquet multipliers.

Figure 5.29 shows the stability regions in the $K_{\phi p} - K_{\phi i}$ space. In this figure, contour lines are presented for different Floquet multipliers to show the different speed of response. From this figure it can be noticed that there is large area in the plane $K_{\phi p} - K_{\phi i}$ for which the speed of response is very similar, so we can select any set of gains $K_{\phi p} - K_{\phi i}$ in this area. However, for practical applications, a large set of gains is not a good choice. A smaller set of gains has an easier implementation, e.g. $K_{\phi p}=0.6$ and $K_{\phi i}=180$.

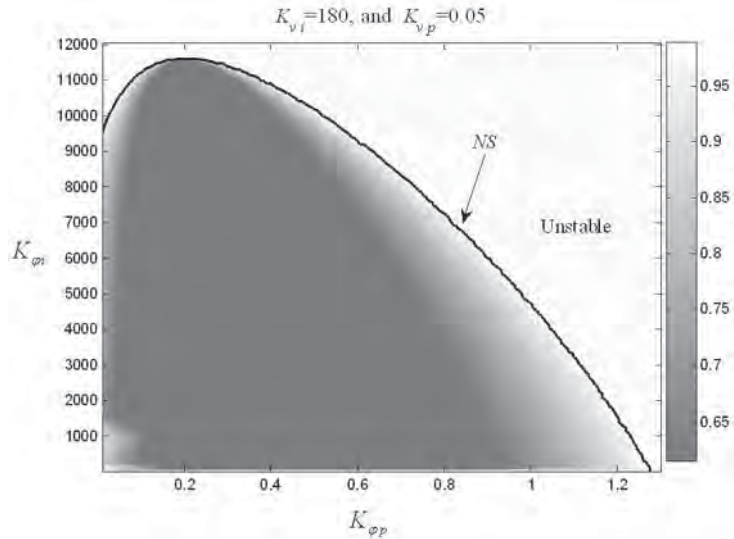


Figure 5.29 Stability regions for the DVR in the $K_{\phi p} - K_{\phi i}$ space.

Now, the stability region in the $K_{vp} - K_{vi}$ plane is shown in Figure 5.30 for the set of gains $K_{\phi p}=0.6$ and $K_{\phi i}=180$ chosen from Figure 5.29. The set of gains for the load voltage controller is selected from the Figure 5.30 as $K_{vp}=0.2$, and $K_{vi}=100$. Thus, the whole set of gains are now selected as $K_{\phi p}=0.6$, $K_{\phi i}=180$, $K_{vp}=0.2$, and $K_{vi}=100$.

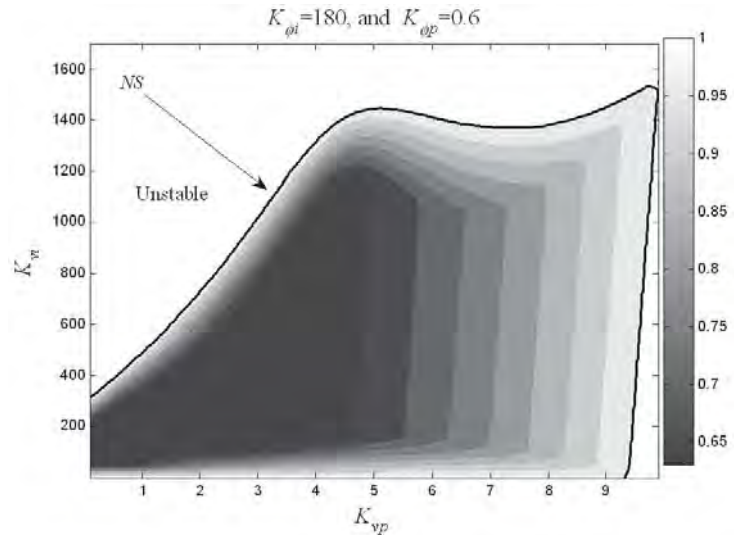


Figure 5.30 Stability regions for the DVR in the $K_{vp} - K_{vi}$ space.

To show the impact of the selected set of gains on the DVR stability, the stability regions in the Thevenin equivalent space are shown in Figure 5.31 for $|V_s|=0.9$ pu in Figure 5.31(a), $|V_s|=1$ pu in Figure 5.31(b), and $|V_s|=1.1$ pu in Figure 5.31(c), respectively. Notice that the stability boundaries have been increased, as compared with those shown in Figure 5.28. The set of gains I are given in Table 3.3, and the set of gains II are $K_{\phi p}=0.6$, $K_{\phi i}=180$, $K_{vp}=0.2$, and $K_{vi}=100$.

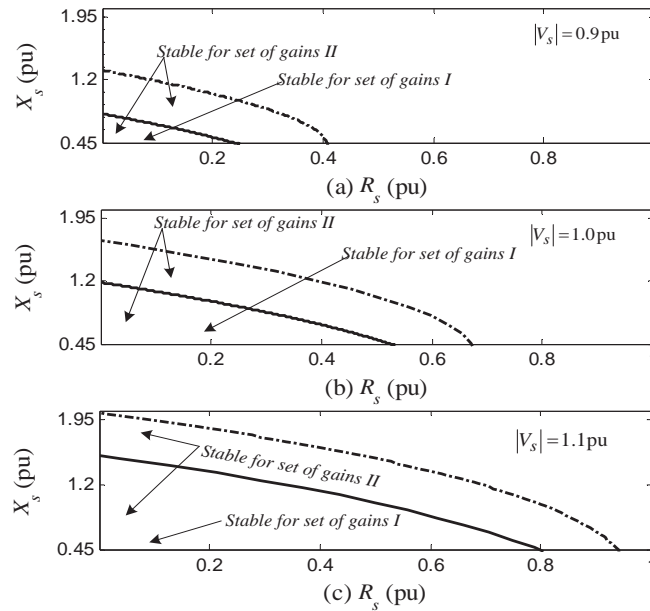


Figure 5.31 Stability regions for the DVR in the $R_s - X_s$ plane for different Thevenin equivalent voltages and different set of gains.

The selected set of gains obtained with the bifurcation analysis improves the stability region and the speed of response of the DVR.

5.4.3 ac Capacitor Impact on the Stability

The main purpose of the ac capacitor filter is to reduce the harmonic content of the injected voltage by the converter. For a low value of X_f , the capacitor current is high, while this current reduces with the increase in the value of X_f . In effect, a reduction of X_f behaves like a short circuit, and the DVR cannot properly compensate, while a large value of X_f makes the filtering inadequate [Ghosh and Jindal 2004]. The value of the ac capacitor filter impacts the filtering performance; besides, this impacts the stability of the DVR. To assess the ac capacitor filter impact on the stability, the stable regions in the Thevenin plane have been compared for three different ac capacitors; this comparison can be seen in Figure 5.32. From this figure, it is easy to notice that the ac capacitor has a negative impact on the stability, since the stable region on the $R_s - X_s$ plane reduces as the ac capacitor capacity becomes larger.

From the results shown in Figure 5.32, it is possible to observe that for a good selection of C_f , two important design specifications have to be taken into account: 1) the THD in load voltage should be within a limit of 5% [Mohan, et al. 1995], and 2) that the stability region should be the maximum possible, since it means that inside of this region the DVR can properly compensate the load voltage. Therefore, we can deduce that the optimum value of C_f is that for which the maximum THD inside of the stable region is 5%. It is important to notice for this particular case, that if the maximum THD is reduced by increasing C_f , then the stable region on the $R_s - X_s$ becomes smaller, which is undesirable for practical purposes.

Figure 5.33 shows the stability region on the $R_s - X_s$ plane for $X_f=21$ pu. In addition, the THD in the load voltage is plotted in this figure as contour lines and it is observed that the THD is within the limits inside of the stable region in the $R_s - X_s$ plane. Thus, from the simulation experiment the ac capacitor is selected as $X_f=21$ pu.

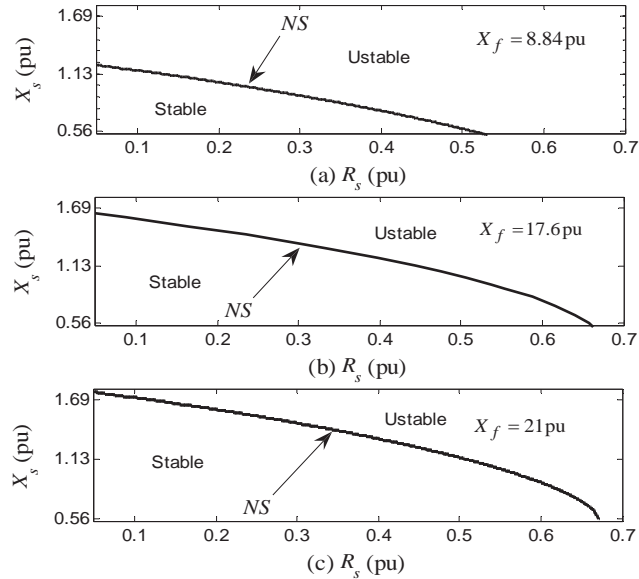


Figure 5.32 Stability regions for the DVR in the $R_s - X_s$ plane for different X_f using the detailed model.

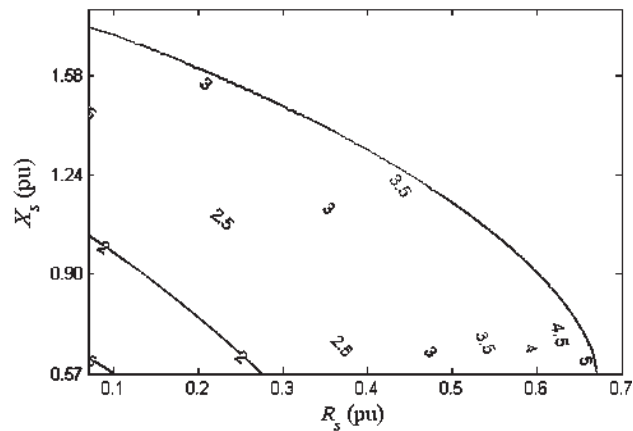


Figure 5.33 Stability regions for the DVR in the $R_s - X_s$ plane for $|V_s|=1$ pu, and $X_f=21$. The contour lines (gray) show the THD (%) in the load voltage.

5.4.4 dc Capacitor Impact on the Stability

The dc capacitor is a very important element in the design of the DVR, as it stores the necessary energy to compensate the load during disturbances. In steady state, the DVR has to provide the active power fluctuation and the reactive power demanded by the system, in order to maintain the voltage at the PCC bus. Thus, the dc capacitor size is important for the compensator performance; e.g. for large capacitances, the stored energy is high;

consequently, the DVR can bear longer and more severe disturbances. This observation suggests that the stable region increases as the dc capacitor size becomes larger. Figure 5.34 shows the stability region in the $X_{dc} - |V_s|$ plane. It can be seen from Figure 5.34 that the capability to compensate voltage sags by the DVR increase as the dc capacitor becomes larger. From this analysis, the dc capacitor size can be selected to suit the load demand, e.g. $X_{dc}=9.2$ pu for this case. It can be seen that the largest size of the dc capacitor is not the best choice. For example, in the Figure 5.34, it is easy to notice that for reactances below $X_{dc}=9.2$ the maximum sag that can be compensated by the DVR does not significantly change, therefore, the dc capacitor size has to be selected using the maximum voltage ripple as an auxiliary criterion of design. In Figure 5.34 contour lines showing the maximum voltage ripple in the dc capacitor are in addition plotted.

It is observed from Figure 5.34 that the maximum voltage ripple in the dc capacitor for $X_{dc}=9.2$ pu is 5% [Mohan, et al. 1995], which remains within limits.

To corroborate the bifurcation diagram shown in Figure 5.34, various time domain simulations were carried-out for different Thevenin voltages. Initially, the system including the DVR is in periodic steady-state with $|V_s|=1$ pu. Then at $t=0.1$ s the Thevenin voltage magnitude is changed from $|V_s|=1$ pu Volts to $|V_s|=0.92$ pu; for this operating point, the DVR properly compensates, as we expected from Figure 5.34. However, when $|V_s|$ is decreased to $|V_s|=0.82$ pu for $t \in [0.3, 2.5)$ s, the electric system becomes unstable and a chaotic solution appears. At $t=2.5$ s $|V_s|$ is increased to $|V_s|=0.86$ pu; for this operating point the DVR correctly compensates. All these changes in the Thevenin voltage are shown in the waveforms of Figure 5.35. The dc capacitor voltage v_{dc} , and the mean magnitude of the load voltage $|V_l|$ are shown in Figure 5.35(a) and Figure 5.35(b), respectively. These observations agree with the bifurcation diagrams shown in Figure 5.34. Also observe that the maximum voltage ripple at the dc capacitor does not exceed 5% in the stable operation of the DVR. Thus, from the conducted experiment the dc capacitor is selected as $X_{dc} = 9.2$ pu .

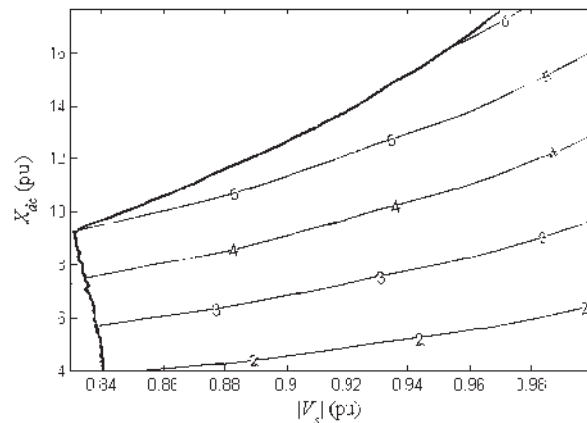


Figure 5.34 Stability regions for the DVR in the $X_{dc} - |V_s|$ (black line), and contour lines showing the maximum voltage ripple (%) in the v_{dc} (gray lines).

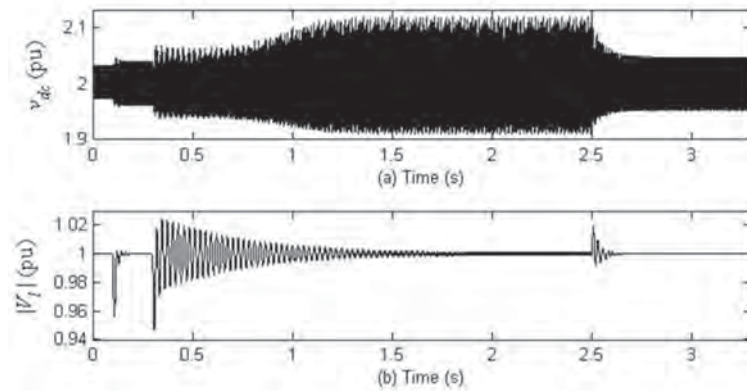


Figure 5.35 Time domain solution. (a) v_{dc} , and (b) $|V_f|$

Figure 5.36 shows how the quasiperiodic solution in the i_{sa} - v_{fa} plane becomes chaotic when $|V_s|$ is changed from 0.82 pu to 0.81 pu. In Figure 5.36(a) the solution in the i_{sa} - v_{fa} for $|V_s|=0.82$ pu; this form describes a quasiperiodic solution. On the other hand, in Figure 5.36(b) the solution in the i_{sa} - v_{fa} plane for $|V_s|=0.81$ pu is shown; this is a chaotic solution. The solutions in Figure 5.36 are illustrated by their Poincaré maps.

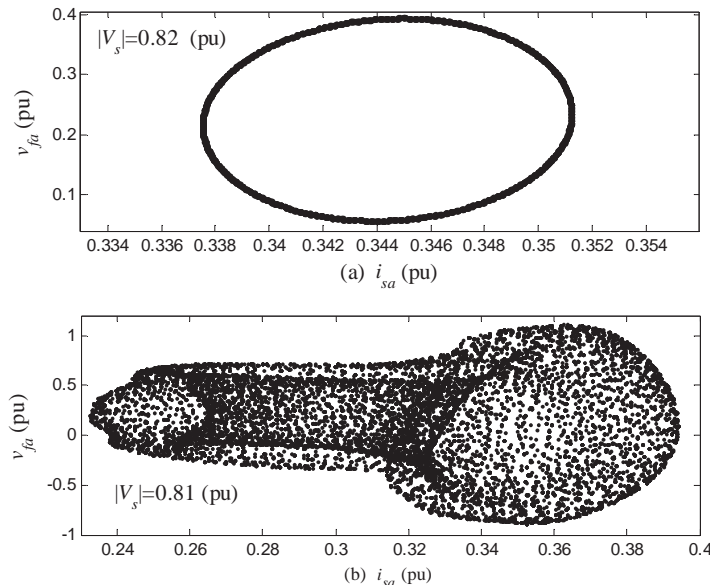


Figure 5.36 Phase portrait for different operating points. (a) $|V_s|=0.82$ pu. (b) $|V_s|=0.81$ pu.

5.4.5 Feasible Solutions of the DVR

The real and positive solutions of (3.61) are the feasible solutions of the DVR. In particular, for the test systems shown in Figure 3.34, the feasible solution in the $R_s - X_s$ plane is limited by R_s . For example, for $|V_s|=1$ pu, $|V_f|=1$ pu, $Z_f=2+j1.8$ pu, the feasible solution in the $R_s - X_s$ plane is limited by $0 \leq X_s \leq \infty$, and $0 \leq R_s \leq 0.69$ pu. Most of these solutions are impractical, since large values of $|V_f|$ are necessary for large values of X_s . In addition, very large values of X_s are not present in a real feeder or transmission line.

In a more realistic case, the power converter capability imposes additional restrictions to the feasible solutions of the DVR. Such restriction is basically associated to the injected saturated voltage when the converter is operating in the nonlinear region, e.g. $m_a > 1$. In the nonlinear region, the harmonic distortion increases in the voltages injected by the converter, which is undesirable. In this investigation, the converter has been only operated in the linear region.

Figure 5.37 shows a comparison between the feasible solution and the stability region in the $R_s - X_s$ plane for $|V_s|=0.9$ pu, $|V_s|=1$ pu, and $|V_s|=1.1$ pu in Figure 5.37(a), Figure 5.37(b), and Figure 5.37(c), respectively. In these Figures, the amplitude modulation index has been also included. An amplitude modulation index of 0.9 has been imposed to the feasible solution.

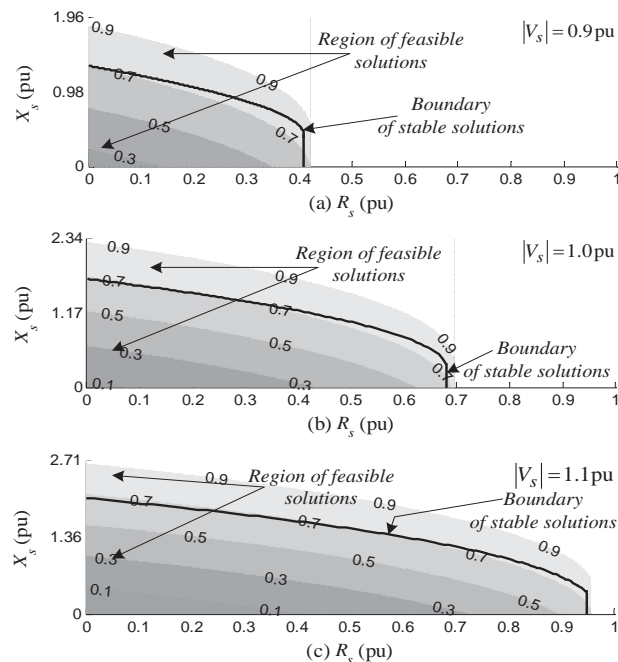


Figure 5.37 Stability and feasible regions for the DVR in the $R_s - X_s$ plane for different Thevenin equivalent voltages and different amplitude modulation indexes.

It can be noticed that the feasible solution, even for an amplitude modulation index of 0.9 is larger than the stability region. However, it has been shown in Figure 5.34 and Figure 5.33 that the stability boundary can be increased if the dc capacitor size is increased and/or the ac filter capacitor size is decreased, respectively. To increase the dc capacitor size increases its price, and to decrease the ac filter capacitor size increases the THD in the load voltage. For these reasons they could not be practical options to increase the stability region.

A comparison between the stability regions in the $R_s - X_s$ plane for different options of ac and dc capacitor sizes are shown in Figure 5.38 in order to illustrate some possible options to increase the stable boundary of the DVR. The shadow region shows the feasible solution in the $R_s - X_s$ plane for different amplitude modulation indexes. In addition, the stability boundary for different sets of dc and ac capacitors is presented. The contour line **A** will be taken as the base case, and shows the stability boundary for $X_f=21$ pu and $X_{dc}=9.2$

pu; this contour line has been also shown in Figure 5.37(b). The contour line **B** shows the stability boundary for $X_f=21$ pu and $X_{dc}=4.6$ pu; it can be observed that the increment of the dc capacitor increases the size of its associated stability boundary. This could be a good option in order to increase the stability boundary, if the price is not a primary concern. The contour line **C** shows the stability boundary for $X_f=42$ pu and $X_{dc}=9.2$ pu; it can be noticed that the stability boundary is also increased as compared with the base case when the ac capacitor size is decreased. It is not a good option to increase the stability boundary, since higher harmonic distortion coming from the converter of the DVR is introduced to the power circuit, unless that the frequency modulation index is increased or a multilevel inverter topology is used [Wang, et al. 2006] [Loh, et al. 2004]. Finally, the contour line **D** shows the stability boundary for $X_f=42$ pu and $X_{dc}=4.6$ pu; it can be noticed that the stability boundary is also increased as compared with the line **C** when the ac capacitor size is decreased.

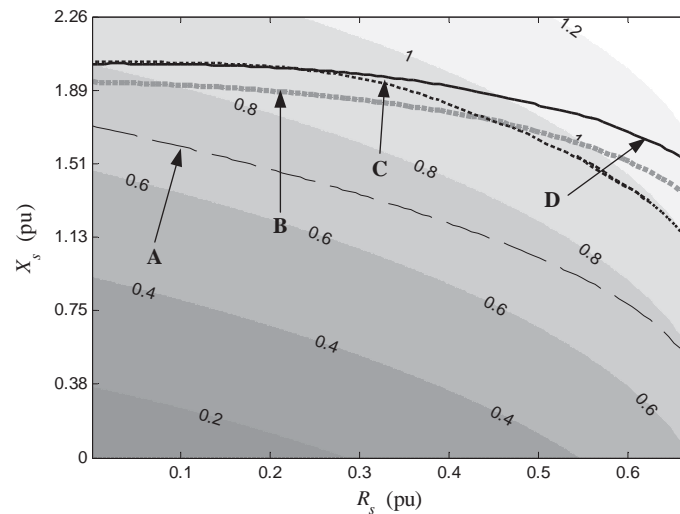


Figure 5.38 Stability and feasible regions for the DVR in the $R_s - X_s$ plane for different ac and dc capacitor sizes.

5.5 Conclusion

Bifurcation theory has been applied to compute the nonlinear oscillations of the DSTATCOM operating in voltage and current control mode, respectively. It allowed delimiting the stable region in which the DSTATCOM is able to keep constant the voltage at the PCC bus. This analysis has been done using the proposed simplified DSTATCOM model based on a state space approach.

Bifurcation diagrams in the Thevenin space have been computed to show the impact on the stability due to voltage variations, as well as Thevenin impedance variations. The variations in the voltage source are associated to voltage sags and voltage swells, as well as disturbances in the network. The connection and disconnection of loads change the Thevenin impedance; it was previously mentioned that the source side impedance is, at best, the Thevenin impedance looking towards the source from the bus controlled.

In addition, the bifurcation diagrams in the gains space have been presented. From this analysis, the set of gains for which the DSTATCOM operates in a stable region can be

obtained. The assessed set of gains for the fastest response of the DSTATCOM has been obtained.

The ac capacitor and dc capacitor impact on the stability has been assessed through bifurcation analysis.

A stability analysis of the DVR based on bifurcation theory using a detailed model of the DVR has been presented. The detailed model used in this analysis includes the switching process in the DVR converter. The bifurcation analysis has been performed using continuation techniques. It has been shown that by moving the system parameters, the system exhibits loss of stability; a Neimark-Sacker bifurcation appears when the fundamental frequency model is used. On the other hand, a Neimark-Sacker bifurcation and supercritical breaking symmetry bifurcation appear when the detailed model of the DVR is used.

It has been shown, through bifurcation analysis, that the widely used fundamental frequency model yields erroneous results if the switching frequency is close to the network transient frequency; the results given by the fundamental frequency model would be reliable if the switching frequency is far from the network transient frequencies.

Bifurcation diagrams in the $R_s - X_s$ plane for different Thevenin voltages have been presented. In addition, the bifurcation diagrams in the $K_{\phi p} - K_{\phi i}$ space and in the $K_{vi} - K_{vp}$ space have been presented. From these bifurcations diagrams in the gain space, the set of gains have been obtained.

The effect on the DVR performance and, the stability of the dc storage capacitor, as well as the ac filter capacitor has been shown. For the case of the dc storage capacitor, it has been demonstrated that the capacitor size has a positive effect on the DVR stability. On the other hand, the ac filter capacitor size has an adverse impact on the DVR stability. In addition, the ac capacitor filter and the dc storage capacitor have been designed using the bifurcation theory.

It has been demonstrated that bifurcation theory can be successfully applied to assess nonlinear oscillations in distribution systems containing DVR. An assessment of qualitative effects of electrical parameters on the stability and on the speed of response of the DVR has been detailed. This analysis allows an effective selection of the DVR parameters to ensure the rated operation condition of the DVR far away from a possible bifurcation. In addition, the bifurcation analysis allowed increasing the stability boundary up to the boundary of feasible solutions.

6 Conclusion

6.1 General Conclusions

Upon the completion of the doctoral research reported throughout the previous chapters of this thesis, the following main conclusions are drawn:

Two efficient Voltage Source Converter models based on Fourier series approach and hyperbolic tangent have been proposed for the six-pulse power converter. The proposed models have been used for the computation of the transient and steady state solution of FACTS devices connected to a power network. An experimental validation of the proposed VSC based on the Fourier approach and the hyperbolic tangent model has been provided in order to demonstrate the potential and accuracy of these models.

The modular SPWM converter blocks have been successfully applied to shunt, series and hybrid FACTS devices. These devices act as distorting sources which interact with the power network.

The response given by the proposed methods has been successfully validated against the solution obtained with the widely accepted digital simulators Simulink and PSCAD/EMTDC, respectively, in all the cases the obtained results were in excellent agreement. In addition, it has been shown through simulations that the proposed models allow significant larger integration steps, as compared with the ideal switch model approach, e.g. for the conducted studies, more than 800 times the integration step needed by Simulink and PSCAD/EMTDC when the Fourier approach was used, and at least 300 times when the hyperbolic tangent method was applied.

These VSCs models have a remarkable advantage over the ideal switch model, since allow to compute the fast periodic steady state solution through a Newton method including the switching process, and as a consequence it is possible to assess the stability of the limit cycle and the impact of the switching on the stability.

The proposed VSCs models can be used in any power electronic device based on SPWM six pulse converters, or even for multilevel converters based on arrangement of six-pulse converters.

A stability analysis of the DSTATCOM in current control mode, the DSTATCOM in voltage control mode, and the DVR based on bifurcation theory has been presented. A state space approach has been developed to represent in the time domain the dynamics of each device connected to the system. A mathematical model based on the energy preservation principle has been developed for the DSTATCOM operating in current control mode, and other for the DSTATCOM in voltage control mode. In addition, a general simplified model

based the smooth functions have been proposed. For the case of the DVR, the VSC models based on the hyperbolic tangent approach has been used.

Bifurcation diagrams in the $L_s - R_s$ plane for different Thevenin voltages have been presented. In addition, the bifurcation diagrams in the $K_{idc} - K_{pdc}$ space and in the $K_{i\beta} - K_{p\beta}$ space have been presented. From these bifurcations diagrams in the gain space, the set of gains for the fastest response of the DSTATCOM has been obtained.

Time domain simulations have been only presented to corroborate the solution obtained from the bifurcation diagrams. From this comparison we have shown that the proposed simplified models retain the nonlinearities, when the switching frequency is far away from the natural frequency of the power system.

The effects on the custom power devices performance and on their stability of the dc storage capacitor, as well as the ac filter capacitor have been presented. It has been shown that the dc capacitor size has a positive effect on the stability. On the other hand, the ac filter capacitor size has an adverse impact on the stability of the DSTATCOM operating in current control mode and on the DVR. The ac filter capacitor size has a positive impact on stability of the DSTATCOM operating in voltage control mode.

It has been demonstrated that bifurcation theory can be successfully applied to assess nonlinear oscillations in distribution systems containing custom power devices. An assessment of qualitative effects of electrical parameters on the stability and on the speed of response of the custom power devices has been achieved. This analysis allows an effective selection of the parameters to ensure the rated operation condition far away from a possible bifurcation.

Newton methods based on a discrete exponential expansion (DEE) approach and enhanced numerical differentiation (END) process have been proposed for the fast periodic steady state solution in the time domain of nonlinear electric networks using a Poincaré map and an extrapolation to the limit cycle process.

The response given by the proposed methodologies have been successfully compared against the periodic steady state solution obtained with the widely accepted digital simulator Power Blockset of SIMULINK for electromagnetic transient studies. In all cases the obtained results have been in close agreement.

6.2 Recommendations for Further Research Developments

Taking as a reference the research work reported in this thesis, the author proposes to proceed in the following directions:

- 1) To apply the proposed voltage source converter models to other FACTS devices. For example an Interline Power Flow Control (IPFC) and the HVDC light.
- 2) To apply the proposed models of the power converter based on the Fourier method and the hyperbolic tangent approach to power electronic devices based on multi-level converters.

- 3) To implement the DEE and the END methods using parallel processing techniques, object oriented programming techniques and sparsity techniques.
- 4) Harmonic state estimation and transient state estimation in the time domain using the DEE and the END methods
- 5) To extend the DEE and END method to compute the periodic steady state solution of large-scale power electric systems decoupling the ODE set in linear and nonlinear sets.
- 6) Harmonic power-flow of power systems in the time domain including flexible ac transmission systems.
- 7) To carry-out the bifurcation analysis of power networks including FACTS devices using the proposed VSCs models to assess the adverse impact of the harmonic distortion introduced by power converters in the power quality and stability.
- 8) To incorporate power flow restrictions to Newton Methods (ND, END, DA, and DEE) to develop a powerful method in the time domain for the computation of the periodic steady state solution of nonlinear power systems, including FACTS and/or Custom Power devices.
- 9) To carry-out stability analysis of power networks with FACTS and Custom power devices including the harmonic distortion injected by the power converters.
- 10) To carry-out stability analysis of Custom Power Parks with the bifurcation theory and continuation methods.
- 11) To carry-out stability analysis of wind generators and wind farms including FACTS and Custom Power devices.
- 12) To assess the impact of distributed generation on power system stability studies through bifurcation theory.

$$\frac{dv_{Pt}}{dt} = \frac{1}{c_{fil}} (i_s - i_s - i_1 - i_p) \quad (\text{A.5})$$

$$\frac{dv_{dc}}{dt} = \frac{1}{c_{dc}} ([S_{sha} \ S_{shb} \ S_{shc}] i_p - [S_{sa} \ S_{sb} \ S_{sc}] i_s) \quad (\text{A.6})$$

where

$$i_s = \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix}, \quad i_p = \begin{bmatrix} i_{pa} \\ i_{pb} \\ i_{pc} \end{bmatrix}, \quad i_1 = \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \end{bmatrix}, \quad i_s = \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix}, \quad v_{Pt} = \begin{bmatrix} v_{Pta} \\ v_{Ptb} \\ v_{Ptc} \end{bmatrix},$$

$$v_{series} = \begin{bmatrix} S_{sa} - \frac{1}{3} \sum_{i=a,b,c} S_{si} \\ S_{sb} - \frac{1}{3} \sum_{i=a,b,c} S_{si} \\ S_{sc} - \frac{1}{3} \sum_{i=a,b,c} S_{si} \end{bmatrix} v_{dc} \quad (\text{A.7})$$

$$v_{shunt} = \begin{bmatrix} S_{sha} - \frac{1}{3} \sum_{i=a,b,c} S_{shi} \\ S_{shb} - \frac{1}{3} \sum_{i=a,b,c} S_{shi} \\ S_{shc} - \frac{1}{3} \sum_{i=a,b,c} S_{shi} \end{bmatrix} v_{dc} \quad (\text{A.8})$$

S_{si} are the switching functions for the series converter, and S_{shi} are the switching functions for the shunt converter. These switching functions can be computed using the proposed approximations presented in Section 3.4.

For the case of the UPFC, v_{series} and v_{shunt} are computed using (A.7) and (A.8), respectively. For the case of the SSSC, v_{series} is computed using (A.7), the shunt bypass is opened and the shunt converter is disconnected from the common dc link. Finally, for the case of the STATCOM, v_{shunt} is computed with (A.8), the series bypass is opened, and the series converter is disconnected from the dc common link.

STATCOM Control

A two-stage control loop scheme is employed for the shunt converter of the STATCOM. This scheme has two objectives: to control the voltage across the dc capacitor, and to regulate the ac voltage of the power system bus where the shunt converter is connected. The control scheme is give in the Figure A.2.

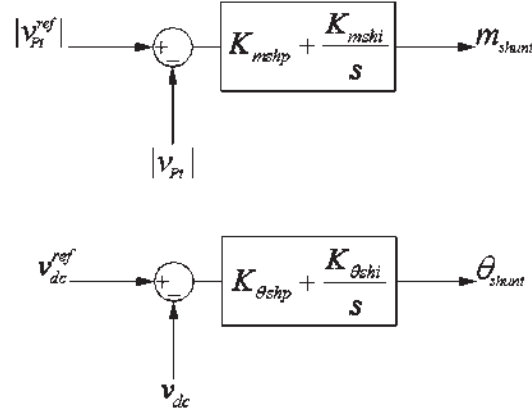


Figure A.2 STATCOM control configuration

For the study case carried-out in Section 3.5.1, the selected gains with real quantities are $K_{\theta shp}=0.0005$, $K_{\theta shi}=0.05$, $K_{mshp}=0.0005$, and $K_{mshi}=1.25$.

UPFC Control

The controller given for the STATCOM is used for the shunt side of the UPFC. The controller proposed in [Fujita, Watanabe and Akagi 2001] is adopted for the series side of the UPFC and is described below.

The reference voltage vector for the series converter is calculated as [Fujita, Watanabe and Akagi 2001],

$$\begin{bmatrix} v_{sd}^{ref} \\ v_{sq}^{ref} \end{bmatrix} = \begin{bmatrix} K_{Sr} & -K_{pSq} - K_{isq}/s \\ K_{pSp} + K_{isp}/s & K_{Sr} \end{bmatrix} \begin{bmatrix} i_{sd}^{ref} - i_{sd} \\ i_{sq}^{ref} - i_{dq} \end{bmatrix} \quad (\text{A.9})$$

where i_{sd}^{ref} and i_{sq}^{ref} are the active and reactive reference currents, v_{sd}^{ref} and v_{sq}^{ref} are reference voltages of the series converter, respectively. The active and reactive reference currents are obtained from the active and reactive power flows and by measuring the voltage at the receiving end.

The magnitude of the voltage at node 1, $|v_{Pt}|$, is computed using (A.10) and (A.11).

$$\theta = \text{atan2} \left(\begin{bmatrix} 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} v_{Pt}^f, \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \end{bmatrix} v_{Pt}^f \right) \quad (\text{A.10})$$

$$|v_{Pt}| = \frac{2}{3} \left[\cos(\theta) \quad \cos\left(\theta - \frac{2\pi}{3}\right) \quad \cos\left(\theta + \frac{2\pi}{3}\right) \right] v_{Pt}^f \quad (\text{A.11})$$

where the superscript f represents the fundamental component.

The active and reactive reference currents are computed using (A.12) and (A.13), respectively.

$$i_{sd}^{ref} = \frac{P_{ref}}{1.5|v_R|} \quad (\text{A.12})$$

$$i_{sq}^{ref} = \frac{Q_{ref}}{1.5|v_R|} \quad (\text{A.13})$$

Here, $| \cdot |$ represents the peak magnitude.

The active and reactive actual currents are computed using (A.14)

$$\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega t - |v_R|) & \cos(\omega t - \frac{2\pi}{3} - |v_R|) & \cos(\omega t + \frac{2\pi}{3} - |v_R|) \\ -\sin(\omega t - |v_R|) & -\sin(\omega t - \frac{2\pi}{3} - |v_R|) & \cos(\omega t + \frac{2\pi}{3} - |v_R|) \end{bmatrix} i_s \quad (\text{A.14})$$

where $|v_R|$ is the phase angle of v_R .

Finally, the amplitude modulation index and the phase angle in the series side of the UPFC are given by (A.15) and (A.16), respectively.

$$m_{series} = \frac{2\sqrt{(v_{sd}^{ref})^2 + (v_{sq}^{ref})^2}}{v_{dc}} \quad (\text{A.15})$$

$$\theta_{series} = \text{atan2}(v_{sq}^{ref}, v_{sd}^{ref}) \quad (\text{A.16})$$

The gain set for the study case presented in Section 3.5.3 is:

$K_{sr}=1$, $K_{psq}=1$, $K_{isq}=250$, $K_{psd}=1$, $K_{isd}=250$, $K_{\theta shp}=0.0008$, $K_{\theta shi}=0.1$, $K_{mshp}=0.001$, and $K_{mshi}=0.8$.

SSSC Control

The SSSC includes the control system shown in Figure A.3.

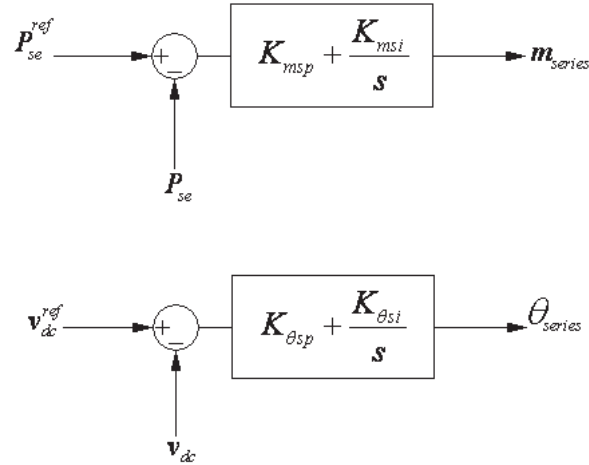


Figure A.3 SSSC control scheme

For the study case carried-out in Section 3.5.2, the selected gains with real quantities are $K_{\theta sp}=0.006$, $K_{\theta si}=1.25$, $K_{msp}=0.0001$, and $K_{msi}=0.008$.

△△△

Remember that for the SPWM technique in the linear range $0 \leq m \leq 1$, the fundamental voltage (at the converter output) is

$$v^f = \frac{v_{dc}}{2} m \cos(\omega t + \theta) \quad (\text{A.17})$$

In particular, the fundamental voltage at the shunt converter output and the series converter output are given by (A.18) and (A.19), respectively.

$$v_{shunt}^f = \frac{v_{dc}}{2} m_{shunt} \cos(\omega t + \theta_{shunt}) \quad (\text{A.18})$$

$$v_{series}^f = \frac{v_{dc}}{2} m_{series} \cos(\omega t + \theta_{series}) \quad (\text{A.19})$$

Appendix B

COMPUTATION OF THE TRANSITION MATRIX IN THE AT METHOD USING THE FOUR-ORDER RUNGE-KUTTA INTEGRATION METHOD

The method to compute the transition matrix in the AT method based on the RK4 method is described next.

The Equation (4.11) can be expressed in terms of the RK4 method as follows:

$$\Delta \mathbf{x}_{k+1} = \prod_{i=1}^N \left(\mathbf{I} + \frac{k_1^i + 2k_2^i + 2k_3^i + k_4^i}{6} \right) \Delta \mathbf{x}_k \quad (\text{B.1})$$

thus,

$$\Phi = \prod_{i=1}^N \left(\mathbf{I} + \frac{k_1^i + 2k_2^i + 2k_3^i + k_4^i}{6} \right) \quad (\text{B.2})$$

where

$$k_1^i = \Delta t_i \mathbf{J}_i \quad (\text{B.3})$$

$$k_2^i = \Delta t_i \mathbf{J}_m (\mathbf{I} + k_1^i / 2) \quad (\text{B.4})$$

$$k_3^i = \Delta t_i \mathbf{J}_m (\mathbf{I} + k_2^i / 2) \quad (\text{B.5})$$

$$k_4^i = \Delta t_i \mathbf{J}_{i+1} (\mathbf{I} + k_3^i) \quad (\text{B.6})$$

$$\mathbf{J}_m = \frac{\mathbf{J}_i + \mathbf{J}_{i+1}}{2} \quad (\text{B.7})$$

$$\mathbf{J}_i = \mathbf{f}_x(t_i, \mathbf{x}_i) \quad (\text{B.8})$$

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